PLASMA PROCESSING APPARATUS WITH TUNABLE ELECTRICAL CHARACTERISTIC

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Nonprovisional Application No. 17/337,067 filed on June 2, 2021, which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] The present invention relates generally to plasma processing, and, in particular embodiments, to apparatuses and methods for plasma processing using a plasma processing apparatus with a tunable electrical characteristic.

BACKGROUND

[0003] Device formation within microelectronic workpieces may involve a series of manufacturing techniques including formation, patterning, and removal of a number of layers of material on a substrate. In order to achieve the physical and electrical specifications of current and next generation semiconductor devices, processing flows enabling reduction of feature size while maintaining structural integrity is desirable for various patterning processes.

[0004] Plasma processes are commonly used to form devices in microelectronic workpieces. For example, plasma etching and plasma deposition are common process steps during semiconductor device fabrication. A combination of source power and bias power may be used to generate and direct plasma during plasma processing. Sequences of direct current (DC) pulses may applied as bias voltage during plasma processes. Short DC pulse trains (i.e. sequences) may be used to increase the flux of high energy ions to a substrate.

[0005] Various parameters such as DC pulse frequency and duty ratios affect ion to radical ratios and other plasma parameters. The DC pulse frequency and duty ratios also affect charge buildup on the biased electrode. Charging of the biased electrode reduces the voltage which undesirably leads to reduced ion flux at the substrate. However, due to the dependence of the ion energy distribution function (IEDF) on the DC pulse frequency and the duty ratios, it is undesirable to manipulate these parameters to reduce substrate charging.

SUMMARY

[0006] In accordance with an embodiment of the invention, a plasma processing apparatus includes a plasma processing chamber, a source power coupling element

configured to generate plasma in an interior of the plasma processing chamber by coupling source power to the plasma processing chamber, a DC pulse generator configured to generate a DC pulse train at a DC pulse frequency, a substrate holder disposed in the interior of the plasma processing chamber, a DC coupling element coupled to the DC pulse generator, a DC current path including the DC coupling element, the plasma, and a reference potential node in a series configuration, the DC coupling element being configured to bias the substrate holder relative to the reference potential node using the DC pulse train, and a capacitive pre-coat layer disposed between the DC coupling element and the plasma. The capacitive pre-coat layer increases the RC time constant of the DC current path according to the DC pulse frequency.

[0007] In accordance with another embodiment of the invention, a plasma processing apparatus includes a plasma processing chamber, a source power coupling element configured to generate plasma in an interior of the plasma processing chamber by coupling source power to the plasma processing chamber, a DC pulse generator configured to generate a DC pulse train including a DC pulse frequency, a substrate holder disposed in the interior of the plasma processing chamber, a DC coupling element coupled to the DC pulse generator, a DC current path including the DC coupling element, the plasma, and a reference potential node in a series configuration, and a tuning circuit coupled between the DC coupling element and the DC pulse generator. The DC coupling element is configured to bias the substrate holder relative to the reference potential node using the DC pulse train. The tuning circuit includes a variable capacitance. The tuning circuit is configured to tune an RC time constant of the DC current path by varying the variable capacitance according to the DC pulse frequency.

[0008] In accordance with still another embodiment of the invention, a method of tuning an electrical characteristic of a plasma processing chamber of a plasma processing apparatus includes determining a capacitance value from a range of capacitance values according to a DC pulse frequency of a DC pulse train to be generated by a DC pulse generator of the plasma processing apparatus, tuning the electrical characteristic by selecting the determined capacitance value using a tuning circuit coupled between a DC coupling element and the DC pulse generator, the tuning circuit including a variable capacitance tunable in the range of capacitance values, and biasing the DC coupling element relative to a reference potential node by generating the DC pulse train at the DC pulse frequency using the DC pulse generator.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0010] FIG. 1 illustrates a schematic timing diagram of an example plasma processing method in accordance with an embodiment of the invention;

[0011] FIG. 2 illustrates qualitative graphs of voltage as a function of time and corresponding qualitative graphs of the ion energy distribution function for several RC time constants at a fixed DC pulse frequency in accordance with an embodiment of the invention;

[0012] FIG. 3 illustrates a schematic diagram of an example plasma processing apparatus comprising a DC current path between a bias power supply and a reference potential node in accordance with an embodiment of the invention;

[0013] FIG. 4 illustrates a schematic diagram of an example plasma processing apparatus comprising an optional capacitive pre-coat layer and an optional resistive pre-coat layer in accordance with an embodiment of the invention;

[0014] FIG. 5 illustrates a schematic diagram of an example plasma processing apparatus comprising a tuning circuit with a variable capacitance in accordance with an embodiment of the invention;

[0015] FIG. 6 illustrates a schematic diagram of an example plasma processing apparatus comprising a tuning circuit along with an optional capacitive pre-coat layer and an optional resistive pre-coat layer in accordance with an embodiment of the invention;

[0016] FIG. 7 illustrates a schematic diagram of an example tuning circuit comprising a single pole switch and a plurality of capacitors in accordance with an embodiment of the invention;

[0017] FIG. 8 illustrates a schematic diagram of an example tuning circuit comprising a single pole switch and a plurality of variable capacitors in accordance with an embodiment of the invention;

[0018] FIG. 9 illustrates a schematic diagram of an example tuning circuit comprising a single pole switch and a plurality of capacitors including fixed capacitors and variable capacitors in accordance with an embodiment of the invention;

[0019] FIG. 10 illustrates a schematic diagram of an example tuning circuit comprising a single pole switch and a plurality of capacitors in accordance with an embodiment of the invention;

[0020] FIG. 11 illustrates a schematic diagram of an example plasma processing apparatus comprising a capacitive pre-coat layer covering an upper electrode, and a tuning circuit coupled to the upper electrode in accordance with an embodiment of the invention; and

[0021] FIG. 12 illustrates an example method of plasma processing in accordance with an embodiment of the invention.

[0022] Corresponding numerals and symbols in the different figures generally refer to corresponding parts unless otherwise indicated. The figures are drawn to clearly illustrate the relevant aspects of the embodiments and are not necessarily drawn to scale. The edges of features drawn in the figures do not necessarily indicate the termination of the extent of the feature.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0023] The making and using of various embodiments are discussed in detail below. It should be appreciated, however, that the various embodiments described herein are applicable in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use various embodiments, and should not be construed in a limited scope.

[0024] DC pulse trains may be useful for creating a large flux of high energy ions at a substrate. For example, DC pulse trains may accelerate ions toward the substrate by causing a voltage differential between the substrate and the plasma. Short DC pulse trains may be applied in an afterglow phase of a plasma as part of a pulsed plasma process (e.g. applying pulsed source and bias power). DC pulse trains may be useful for a variety of applications such as gate etching, patterning, high-aspect ratio contact (HARC) etching, memory fabrication.

[0025] However, the flux and energy of the ions is dependent on the ability to maintain the voltage differential between the plasma and the substrate surface. Charging at the substrate results in a reduction of this voltage differential and therefore lowers the effectiveness of an applied voltage over time. Therefore, the effects of each DC pulse must be controlled at the electrode (e.g. at a dielectric-covered electrode).

[0026] Conventional DC pulse implementations have various drawbacks. Difficulties arise due to the differences between the optimal parameter values (e.g., pulse length, pulse frequency, duty ratio) for a given process and the parameter values needed to maintain a plasma sheath. For instance, it may be undesirable to alter the DC pulse frequency and duty ratio for a given process even though charging might be reduced by doing so. Therefore, a

plasma processing apparatus capable of reducing the rate of substrate charging without varying the DC pulse frequency or duty ratios may be desirable.

[0027] The RC electrical characteristic of the plasma processing chamber (i.e. as seen by a DC power supply) significantly impacts the charging and discharging of the substrate during the application of a DC bias voltage. Consequently, the period that a sheath voltage can be maintained is determined in large part by the RC time constant τ of the chamber. It is generally desirable to maintain a sheath voltage through as much of each DC pulse as possible. The DC voltage response at the substrate during application of DC pulse trains can be controlled for arbitrary pulse lengths, pulse frequencies, and duty ratios by controlling the RC time constant τ.

[0028] The RC time constant τ can be tuned by altering the resistance and/or the capacitance of a DC current path between a DC power supply and a reference potential (e.g. a ground potential such as the grounded wall of a plasma processing chamber). Adjusting the capacitance may be accomplished by adding one or more capacitors between a DC coupling element (e.g. an electrostatic chuck) and the DC power supply. Additionally or alternatively, a capacitive pre-coat layer may be formed over the DC coupling element resulting in a large increase in capacitance. Similarly, the resistance can be adjusted by applying a resistive pre-coating to various inner surfaces of the plasma processing chamber or by adding resistors at various points along the DC current path.

[0029] A tuning circuit may be included between a DC pulse generator and the DC coupling element. The tuning circuit may include various capacitors such as fixed and variable capacitors. The capacitors may be arranged as banks of capacitors in parallel. Individual capacitors, banks of capacitors or other subsets of the capacitors may be selectable using one or more switches. A short circuit path between the DC pulse generator and the DC coupling element may also be included and selectable by the one or more switches.

[0030] The plasma processing apparatus and method of plasma processing described herein may advantageously give DC pulse train processes more margin and efficacy. For example, at low DC pulse frequencies, substrate charging may reduce or eliminate the desired effects of the DC pulse train. The apparatuses and methods described herein may advantageously decrease the effects of substrate charging at lower DC pulse frequencies.

[0031] The reduced substrate charging may in turn provide the benefit of allowing control over the IEDF. In particular, the ion energy spread may be reduced, average ion energy may be increased, and high energy ion flux at the substrate may be increased over conventional DC pulse train processes. Control over the energy distribution and the ion

energy flux may be desirable in order to approach an ideal monoenergetic flux of appropriate magnitude for a given process.

[0032] Various embodiments described herein may advantageously allow an electrical characteristic of the plasma processing apparatus to be tuned to different DC pulse frequencies. For example, a tuning circuit including a variable capacitance may be utilized to select an appropriate capacitance (and/or resistance) in order to tune the electrical characteristic of a plasma processing chamber as seen by a bias power supply according to a desired DC pulse frequency.

[0033] Embodiments provided below describe various apparatuses and methods for plasma processing, and in particular, apparatuses and methods for plasma processing that include a tunable electrical characteristic. The following description describes the embodiments. An example schematic timing diagram of an embodiment plasma processing method is described using FIG. 1. Various qualitative graphs of voltage as a function of time and corresponding qualitative IEDF graphs corresponding to an embodiment plasma processing method at a given DC pulse frequency are described using FIG. 2. FIG. 3 is used to describe an embodiment plasma processing apparatus. Several other embodiment plasma processing apparatuses are described using FIGS. 4–6. An embodiment tuning circuit is described using FIG. 7. Three more embodiment tuning circuits are then described using FIGS. 8–10. Another embodiment plasma processing apparatus is described using FIG. 11. An embodiment method is described using FIG. 12.

[0034] FIG. 1 illustrates a schematic timing diagram of an example plasma processing method in accordance with an embodiment of the invention.

[0035] Referring to FIG. 1, a schematic timing diagram 100 illustrates the application of source power (SP) and bias power applied as DC voltage in a plasma processing apparatus. An SP pulse 111 and a DC pulse train 115 comprising a sequence of DC pulses 113. The SP pulse 111 and the DC pulse train 115 may be one cycle of a repeated process with SP pulse period T_{SP}. Each SP pulse 111 has an SP pulse duration t_{SP} indicating the length of time that the source power is continuously applied in a given cycle. An SP duty ratio D_{SP} can be defined as t_{SP}/T_{SP}. Similarly, each DC pulse has a DC pulse duration t_{DC} and a DC pulse period T_{DC} with a DC duty ratio D_{DC} being defined as t_{DC}/T_{DC}. As illustrated, multiple DC pulses 113 (i.e. multiple periods T_{DC}) are applied in every SP pulse period T_{SP}. A DC duty ratio of 50% ($D_{DC} = 0.5$) is shown, but both D_{DC} and D_{SP} may be any value between 0 and 1.

[0036] The source power may be alternating current (AC) power. For example, the source power may be radio frequency (RF) power with SP frequency f_{SP}. A delay t_d may be included between the application of source power and the application of bias power in the

form the DC pulse train 115. In some cases, a delay may also be included between the DC pulse train 115 and a subsequent SP pulse 111.

[0037] The DC pulse train 115 is applied at a DC pulse frequency f_{DC} corresponding to the rate that successive DC pulses 113 are applied (i.e. $f_{DC} = 1/T_{DC}$). The DC pulse frequency f_{DC} is less than the SP frequency f_{SP}. In various embodiments, f_{DC} is less than about 1000 kHz. In some embodiments, f_{DC} is less than about 20 kHz and may be on the order of 1 kHz or lower. The DC pulse period T_{DC} of f_{DC} (T_{DC} = 1 μs when f_{DC} = 1000 kHz, T_{DC} = 50 μs when f_{DC} = 20 kHz, and so on).

[0038] Even at the higher DC pulse frequencies (e.g. above 100 kHz) the DC pulse train 115 differs from application of low frequency RF power because the bias power does not oscillate, but instead is removed for a fraction of each cycle equal to $1-D_{DC}$. However, the various benefits of applying short DC pulse trains may be somewhat diminished as f_{DC} is increased beyond 1000 kHz (e.g. due to rise and fall rate limitations).

[0039] The SP pulse period T_{SP} is much longer than the DC pulse period T_{DC}. For example, the SP pulses 111 may be applied at a frequency between about 1 kHz and about 10 kHz in one embodiment although it can be much lower. This corresponds to T_{SP} being between about 10 μs and about 1 ms. Consequently, t_{SP} may range from about 5 μs to about 25 μs or longer.

[0040] It should be noted that that relative power levels of the source power and bias power are not indicated on the timing diagram 100. Similarly, the relative pulse lengths and the number of DC pulses in an SP period are also not represented by the timing diagram 100 in order to improve comprehension. That is, as implicitly indicated by the example frequencies and pulse lengths above, it is not uncommon for more than 50 DC pulses to occur in a given SP period.

[0041] FIG. 2 illustrates qualitative graphs of voltage as a function of time and corresponding qualitative graphs of the ion energy distribution function for several RC time constants at a fixed DC pulse frequency in accordance with an embodiment of the invention.

[0042] Referring to FIG. 2, qualitative graphs 200 demonstrate the effects of varying the time constant τ while maintaining a DC pulse frequency f_{DC} of 400 kHz and a 50% duty ratio (D_{DC} = 0.5). Throughout the voltage graphs of the top row, the rod electrode response (e.g. of the DC coupling element) remains constant and is shown as dashed curve 120. As τ is increased from τ = 0.2 μs to τ = 20 μs, the voltage response at a substrate surface is shown as solid curves 121–125. The voltage at the substrate surface in this example is shown as negative, but it may also be positive depending on the configuration of the reference potential and the supplied bias power.

[0043] As shown by curve 121, at τ = 0.2 μs the voltage at the substrate surface initially decreases with the rod electrode response, but then sharply increases due to charging before even reaching the minimum voltage of the rod electrode. This results in a steep return slope that diverges dramatically from the approximate square wave response of the rod electrode. At τ = 1 μs (curve 122) the slope lessens, but the voltage still doesn't reach the minimum voltage of the rod electrode and voltage overshoot at the rising edge of the rod voltage becomes more pronounced. At τ = 5 μs the slope of the bottom of the surface curve 123 is beginning to approach the flat square waveform of the rod voltage. The surface voltage reaches the minimum voltage and only increases about 15% over the 1.25 μs duration of the DC pulse.

[0044] As τ is increased to 10 μs and then further to 20 μs, the slope continues to flatten out, but with diminishing returns as the slope nearly mirrors the rod response. Consequently, the slope at the bottom of curve 124 is very similar to the slope at the bottom of curve 125. On the other hand, the voltage overshoot changes more dramatically from τ = 10 μs to τ = 20 μs as it begins to also approach the rod electrode response.

[0045] IEDF graphs 131–135 show the resulting IEDF at the substrate surface and correspond with curves 121–125 respectively. Due to the brief time that the surface spends at a negative voltage the IEDF for τ = 0.2 μs shown in graph 131 has low energy (~700 eV) and a large spread (indicated by the double-sided arrows). Similarly, at τ = 1 μs (graph 132) the ion energy is increased overall, but still only reaches about 950 eV with a ~500 eV spread. Lower ion energy can be disadvantageous since more voltage is needed to reach a desired ion energy. However, large energy spread can be even more undesirable as many of the ions reaching the substrate will not have the energy needed to produce the required effect. This may result in a drop in process efficiency and can render some processes impractical.

[0046] In contrast, graph 133 shows that the ion energy reaching 1 keV at τ = 5 μs matches the applied voltage of -1 kV. Additionally, the flattening of the slope results in a much smaller energy spread of ~200 eV. Graphs 134 and 135 illustrate that as τ is increased to 10 μs and 10 μs the energy spread continues to decrease and the number of energetic ions increases.

[0047] The period T_{DC} for f_{DC} = 400 kHz is 2.5 μs. As can be seen from the above analysis, τ = 5 μs provides various advantages in the surface voltage and the resulting IEDF. As 5 μs is double the period of 2.5 μs, a generally beneficial target for τ given f_{DC} might be $\tau \geq 2/f_{DC}$. In words, the RC time constant is at least double the inverse of the DC pulse frequency. This target gives τ = 2 μs for f_{DC} = 1000 kHz and τ = 100 μs for f_{DC} = 20 kHz, as examples.

[0048] It should be noted, however, that this target may or may not accurately describe the desired τ depending on the specific details of a given application. For example, increasing τ at a given f_{DC} continuously produces beneficial effects from the beginning, and not just upon reaching a particular target. Therefore, some applications may utilize a $\tau < 2/f_{DC}$ (e.g. if $2/f_{DC}$ is impractical). Similarly, τ may often be in the vicinity of $2/f_{DC}$, but may also far exceed this value in applications where a near perfect square wave response at the substrate surface is desirable.

[0049] The duty ratio D_{DC} may impact the target for τ. For example, the IEDF spread may increase as D_{DC} becomes larger (> 0.5) and decrease as D_{DC} becomes smaller (> 0.5). Consequently, it may be desirable to have a higher τ for higher D_{DC} and a lower τ for lower D_{DC} compared to the target for τ at 50% duty ratio in a given plasma process.

[0050] FIG. 3 illustrates a schematic diagram of an example plasma processing apparatus comprising a DC current path between a bias power supply and a reference potential node in accordance with an embodiment of the invention. The plasma processing apparatus of FIG. 3 may be configured to perform plasma processing methods as described herein, such as according to the timing diagram of FIG. 1, for example.

[0051] Referring to FIG. 3, a plasma processing apparatus 300 includes a plasma processing chamber 302 coupled to a source power supply 307 and a bias power supply 309. The source power supply 307 is configured to generate plasma 306 in an interior 303 of the plasma processing chamber 302. The source power supply 307 may generate a capacitively coupled plasma (CCP) (as in FIG. 11 for example), an inductively coupled plasma (ICP), a surface wave plasma (SWP), and others. For example, the source power may be coupled to a helical resonator antenna that generates plasma 306 in the plasma processing chamber 302.

[0052] In this schematic example, the source power supply 307 is coupled to the top of the plasma processing chamber 302 and the bias power supply 309 is coupled to a substrate holder 304 in the interior 303 of the plasma processing chamber 302, but other configurations are also possible. The substrate holder 304 is configured to support a substrate 305. For example, the substrate holder 304 may be an electrostatic chuck (ESC). Alternatively, the substrate holder may be a vacuum chuck or other suitable support structure.

[0053] A DC pulse generator 308 is coupled between the bias power supply 309 and the substrate holder 304. The DC pulse generator 308 is configured to generate a DC pulse train at a DC pulse frequency. For example, the DC pulse generator 308 in combination with the bias power supply 309 may be configured to apply a DC pulse train to the substrate holder as shown in the timing diagram 100 of FIG. 1.

[0054] A reference potential node 345 is coupled to the plasma processing chamber 302. In one embodiment, the reference potential node 345 is coupled to a wall of the plasma processing chamber 302 as shown. The reference potential node 345 is a ground connection in one embodiment. The reference potential node 345 creates a DC current path 340 between the bias power supply 309 and the reference potential node 345. The behavior of the DC current path 340 may be modeled as including a resistive component 341 and a capacitive component 343.

[0055] The plasma 306 itself supplies a conductive portion of the DC current path 340. If should be noted that extent of the dashed boundary of plasma 306 is drawn as stopping short of the walls of the plasma processing chamber 302 and the substrate holder 304/substrate 305 for readability purposes only. That is, in reality the plasma 306 extends to and interfaces with the walls of the plasma processing chamber 302, the substrate holder 304, and the substrate 305.

[0056] Further, it should be recognized that this simplified model is conceptual. The actual current paths that contribute to the resistive component 341 and capacitive component 343 may be much more complicated than depicted. That is, plasma current may travel along all surfaces of the chamber. The chamber surfaces may have inductive, resistive, and capacitive components that contribute to the overall behavior of the circuit. Many other contributory sources of the resistive component 341 and capacitive component 343 may also be present (many of which will be discussed in the following).

[0057] The resistive component 341 and the capacitive component 343 of the DC current path 340 contribute to the electrical characteristics of the plasma processing chamber 302 as seen by the bias power supply 309. In this simplified model, the DC current path 340 is a series RC circuit with a time constant τ equal to RC where R is the resistance of the resistive component 341 and C is the capacitance of the capacitive component 343. As previously described in reference to FIG. 2, tuning the time constant τ may improve the voltage response at the substrate 305 and advantageously result in less ion energy spread, higher ion energy, and increased ion flux at the substrate 305.

[0058] Of course, several physical components may contribute to one or both of the resistive component 341 and the capacitive component 343. As will be apparent from the subsequent description, although the locations of the resistive component 341 and the capacitive component 343 may represent the positions of some corresponding physical components, the specific locations are also variable within the plasma processing apparatus.

[0059] FIG. 4 illustrates a schematic diagram of an example plasma processing apparatus comprising an optional capacitive pre-coat layer and an optional resistive pre-coat

layer in accordance with an embodiment of the invention. The plasma processing apparatus of FIG. 4 may be a specific implementation of other plasma processing apparatuses described herein such as the plasma processing apparatus of FIG. 3, for example. Similarly labeled elements may be as previously described.

[0060] Referring to FIG. 4, a plasma processing apparatus 400 includes a substrate holder 404 disposed in an interior 403 of a plasma processing chamber 402 coupled to a source power supply 407 configured to generate plasma 406. A bias power supply 409 is coupled to a DC pulse generator 408 which is in turn coupled to a DC coupling element 453 disposed in the substrate holder 404.

[0061] It should be noted that here and in the following a convention has been adopted for brevity and clarity wherein elements adhering to the pattern [x10] may be related implementations of a plasma processing chamber in various embodiments. For example, the plasma processing chamber 402 may be similar to the plasma processing chamber 302 except as otherwise stated. An analogous convention has also been adopted for other elements as made clear by the use of similar terms in conjunction with the aforementioned three-digit numbering system.

[0062] A reference potential node 445 is coupled to a wall of the plasma processing chamber 402. A DC current path is created from the bias power supply 409, through the DC coupling element 453 and the plasma 406, and to the reference potential node 445.

[0063] The substrate holder 404 is configured to support a substrate 405. A capacitive pre-coat layer 444 may be disposed on an upper surface of the substrate holder 404 between the substrate holder 404 and the substrate 405. However, other configurations are possible. In some embodiments, the capacitive pre-coat layer 444 may also be omitted (e.g. in favor of alternatives or in implementations that only utilize additional resistive components).

[0064] The capacitive pre-coat layer 444 increases the capacitance of the DC current path (functioning as a capacitive component). For example, the capacitance of the capacitive pre-coat layer 444 may be written as $C = \varepsilon A_C / l_C$ where ε is the permittivity, A_C is the area, and l_C is the thickness of the capacitive pre-coat layer 444. While many configurations are possible and will depend on the specifics of a given application, one example set of values may be $\varepsilon = 6$ nF/m, $A_C = (100\text{ mm})^2$, and $l_C = 600$ μm which yields a capacitance C of 100 nF.

[0065] For a given substrate size (e.g. wafer size), A may remain constant while the permittivity ε (i.e. relative permittivity/dielectric constant) and the thickness l_C may be varied to achieve the desired capacitance C. For applications involving substrates of different sizes (e.g. larger wafers), A may impact the choice of ε and l_C by increasing the

capacitance. In some cases higher or lower dielectric constant materials may be needed to ensure appropriate capacitive pre-coat layer thicknesses.

[0066] The capacitive pre-coat layer 444 comprises a dielectric material in various embodiments and is a ceramic material in some embodiments. The capacitive pre-coat layer 444 may comprise silicon, and comprises silica (SiO_2) in one embodiment. In another embodiment, the capacitive pre-coat layer 444 comprises yttria (Y_2O_3).

[0067] However, a variety of dielectric materials may be suitable for use as the capacitive pre-coat layer 444. As the aforementioned equation indicates, utilizing a material with a higher or lower dielectric constant simply requires increasing or decreasing the thickness l_C accordingly. Other consideration such as process compatibility, potential dielectric breakdown, and other material properties may also be taken into consideration.

[0068] It is recognized that the dielectric constant of a given material depends on a variety of factors. For example, a person skilled in the art would recognize that the dielectric constant is frequency-dependent. In the context of this disclosure, the dielectric constant (and by extension the permittivity) in the capacitance equation is assumed to be considered under the application frequency operating conditions (e.g. DC pulse frequency). It is assumed, in view of the description herein, that a person skilled in the art would be capable of making appropriate adjustments to the thickness of the capacitive pre-coat layer based on the various specifics of a given application.

[0069] A resistive pre-coat layer 442 of thickness l_R may be included on surfaces of the interior 403 of the plasma processing chamber 402. Although here the resistive pre-coat layer 442 is included on surfaces of the plasma processing chamber 402, other configurations are also possible (e.g. depending on the location and configuration of the reference potential node 445). In some embodiments, the resistive pre-coat layer 442 may be omitted (e.g. in favor of alternatives or in implementations that only utilize additional capacitive components).

[0070] Similar to the capacitive pre-coat layer 444 discussed above, the resistive properties of the resistive pre-coat layer 442 increases the resistance of the DC current path (functioning as a resistive component). The geometry of the plasma processing chamber 402 impacts the resistance R of the resistive pre-coat layer 442. For example, the resistance $R = \rho l/A_R$ where ρ is the resistivity, A_R is the cross-sectional area perpendicular to the direction of DC current flow, and l is the length of the resistive pre-coat layer 442 in the direction of the DC current flow. Although the resistive pre-coat layer 442 is only shown covering the vertical sides of the plasma processing chamber 402 it should be understood

that other surfaces such as top surfaces of the plasma processing chamber 402 or side surfaces of the substrate holder 404 may also be covered.

[0071] Assuming that the current travels along the surfaces of the plasma processing chamber 402, A_R may be approximated as $2\pi r \times l_R$ where r is the radius of the plasma processing chamber 402 (for a cylindrical chamber, but any suitable chamber shape may be used). The length l is then the average distance that the current must travel to reach the reference potential node. As one might expect, many configurations are possible and will depend on a variety of specific factors for a given application. One example set of values may be $\rho = 10^{-5}\ \Omega\cdot$m, $A_R = 2\pi(0.15\text{ m})(100\text{ nm}) \approx 10^{-7}$ m^2, and $l = 0.1$ m which yields a resistance R of about 1 kΩ.

[0072] Using the capacitive pre-coat layer 444 and the resistive pre-coat layer 442 values of τ that significantly improve voltage response at the surface of the substrate 405 may advantageously be attainable for a wide range of frequencies. For example, for $C = 100$ nF and $R = 1$ kΩ, $\tau = 100$ μs (= 2/20 kHz). Doubling C and R results in $\tau = 400$ μs corresponding to $f_{DC} = 5$ kHz. Although certain practical limitations may exist regarding the maximum values of C and R, the effects of charging may be reduced over a large portion of the duration of each DC pulse at advantageously low DC pulse frequencies f_{DC}.

[0073] The resistive pre-coat layer 442 comprises a resistive material in various embodiments. In one embodiment, the resistive pre-coat layer 442 comprises amorphous carbon (aC). In another embodiment, the resistive pre-coat layer 442 comprises graphitic carbon. The resistive pre-coat layer 442 may also comprise graphitic carbon-based materials. Additionally, the resistive pre-coat layer 442 may also comprise a silicon-like material, or a silica-like material, as well as others. Since the resistive pre-coat layer 442 is exposed to the plasma 406 and the substrate 405, the choice of material may be impacted by process compatibility. For example, carbon-based resistive pre-coat layers may be compatible with Si and SiO_2 etching processes.

[0074] FIG. 5 illustrates a schematic diagram of an example plasma processing apparatus comprising a tuning circuit with a variable capacitance in accordance with an embodiment of the invention. The plasma processing apparatus of FIG. 5 may be a specific implementation of other plasma processing apparatuses described herein such as the plasma processing apparatus of FIG. 3, for example. Similarly labeled elements may be as previously described.

[0075] Referring to FIG. 5, a plasma processing apparatus 500 includes a substrate holder 504 configured to support a substrate 505 and disposed in an interior 503 of a plasma processing chamber 502 coupled to a source power supply 507 that is configured to generate

plasma 506. A tuning circuit 501 is coupled between a DC pulse generator 508 and a DC coupling element 553 disposed in the substrate holder 504. A bias power supply 509 is coupled to the DC pulse generator 508. A reference potential node 545 is coupled to the plasma processing chamber 502.

[0076] The tuning circuit 501 has a variable capacitance. That is, the capacitance of the tuning circuit 501 may be varied in order to tune an electrical characteristic if the plasma processing chamber 502. In one embodiment, the electrical characteristic is the time constant τ of a DC current path between the bias power supply 509 and the reference potential node 545. The capacitance of the tuning circuit 501 may be tuned manually or automatically, and during or in between operation of the plasma processing apparatus 500. The capacitance of the tuning circuit 501 may be selected mechanically, electronically, electromechanically, or with any other suitable selection mechanism.

[0077] The tuning circuit 501 may also include static or variable resistive components. In some cases it may be desirable to incorporate such additional resistive components between the substrate 505 and the reference potential node 545 rather than between the substrate 505 and the bias power supply 509 in order to prevent an unnecessary voltage drop between the substrate 505 and the bias power supply 509.

[0078] FIG. 6 illustrates a schematic diagram of an example plasma processing apparatus comprising a tuning circuit along with an optional capacitive pre-coat layer and an optional resistive pre-coat layer in accordance with an embodiment of the invention. The plasma processing apparatus of FIG. 6 may be a specific implementation of other plasma processing apparatuses described herein such as the plasma processing apparatus of FIG. 3, for example. Similarly labeled elements may be as previously described.

[0079] Referring to FIG. 6, a plasma processing apparatus 600 includes a substrate holder 604 configured to support a substrate 605 and disposed in an interior 603 of a plasma processing chamber 602. A tuning circuit 601 is coupled between a DC pulse generator 608 and a DC coupling element 653 disposed in the substrate holder 604. A bias power supply 609 is coupled to the DC pulse generator 608. A reference potential node 645 is coupled to the plasma processing chamber 602.

[0080] A source power supply 607 that is configured to generate plasma 506 is coupled to a source power coupling element 651. In one embodiment, the source power coupling element 651 is an inductive coupling element that couples source power to the plasma processing chamber 602 through an insulator 655 (as shown), but other configurations are possible.

[0081] A capacitive pre-coat layer 644 may be disposed on an upper surface of the substrate holder 604 between the substrate holder 604 and the substrate 605. A resistive pre-coat layer 642 may be included on surfaces of the interior 603 of the plasma processing chamber 602. In some embodiments, the capacitive pre-coat layer 644 or the resistive pre-coat layer 642 may be omitted.

[0082] In embodiments where both the tuning circuit 601 and the capacitive pre-coat layer 644 are included, the total capacitance C of the DC current path between the bias power supply 609 and the reference potential node 645 is a combination of both capacitive components. Since the tuning circuit 601 is in series with the capacitive pre-coat layer 644, $C = (1/C_{\text{fixed}} + 1/C_{\text{tuning}})^{-1}$.

[0083] Due to the form of the series capacitor equation, C will always be less than C_{fixed} and will approach C_{fixed} as C_{tuning} becomes very large. In some cases, the tuning circuit 601 may include a short circuit option that does not add capacitance allowing C to equal C_{fixed} when selected. Since even values of C_{tuning} far exceeding C_{fixed} (e.g. 10 times) still only result in C being 91% of C_{fixed}, if a C equal to C_{fixed} is desired, the tuning circuit 601 may be bypassed using the short circuit option.

[0084] FIG. 7 illustrates a schematic diagram of an example tuning circuit comprising a single pole switch and a plurality of capacitors in accordance with an embodiment of the invention. The tuning circuit of FIG. 7 may be a specific implementation of other tuning circuits described herein such as the tuning circuits of FIGS. 5 and 6, for example. Similarly labeled elements may be as previously described.

[0085] Referring to FIG. 7, a tuning circuit 701 includes a first tuning input/output 757 (e.g. for coupling to a DC coupling element) and a second tuning input/output 759 (e.g. for coupling to a DC pulse generator). The tuning circuit 701 further includes a plurality of capacitors 760 which may include fixed capacitors 762 as shown. In various embodiments, the fixed capacitors 762 are high reliability capacitors. In some embodiments, some or all of the fixed capacitors 762 are vacuum capacitors. In some embodiments, some or all of the fixed capacitors 762 are ceramic capacitors.

[0086] A first single pole switch 771 includes a single pole (input) coupled to the first tuning input/output 757 and at least one throw (output) coupled to a subset of the plurality of capacitors 760. An optional second single pole switch 772 may be coupled between the subset of the plurality of capacitors 760 and the second tuning input/output 759 (e.g. to further isolate the current paths that are not selected from the selected current path). The locations of the first single pole switch 771 and the optional second single pole switch 772

may be switched. Optionally, a short circuit path 764 is also included between the first tuning input/output 757 and the second tuning input/output 759.

[0087] The first single pole switch 771 (and the optional second single pole switch 772) is a mechanical switch in some embodiments. In one embodiment, the mechanical switch is an electromechanical switch. In other embodiments, other suitable switches may be used such as electrical switches. However, it should be noted that care should be taken to avoid parasitics and dielectric breakdown due to application of high voltage.

[0088] In one embodiment, the first single pole switch 771 is a single pole multiple throw switch (as illustrated) including multiple outputs coupled to multiple subsets of the plurality of capacitors 760. In another embodiment, the first single pole switch 771 is a single pole single throw switch and the tuning circuit 701 includes additional single pole single throw switches coupled to the plurality of capacitors. Other combinations of single pole switches are of course possible.

[0089] The plurality of capacitors 760 may be arranged as banks of capacitors 763. In one embodiment, the banks of capacitors 763 are physical groupings of separate capacitors. One (or two if the optional switch is included) single pole multiple throw switch may be utilized to select between banks of capacitors completely isolated from one another. In another embodiment, the banks of capacitors 763 are logical groupings (e.g. some or all of the capacitors are used in more than one logical bank).

[0090] The subsets of the plurality of capacitors 760 may be mutually exclusive. However, using the same capacitors in more than one subset may reduce the number of capacitors needed to achieve a given variable capacitance range, but may also increase the complexity of the tuning circuit or allow parasitic currents within the tuning circuit. In one specific example, the first single pole switch 771 is a rotary switch with outputs coupled to n fixed capacitors 762. The rotary switch has $n + 1$ positions that include a position for coupling each number of capacitors from 1 to n and a position coupling zero coupled capacitors (short circuit path 764). A variation omits the short circuit path 764 and includes only n positions.

[0091] In another specific example, the capacitors are arranged in n banks of capacitors that each include 2^m capacitors where m ranges from 0 to $n - 1$. A number n of single pole single throw switches may then be used to select a combination of banks resulting in 1 to $n - 1$ coupled capacitors. If the short circuit path 764 is included, an additional single pole single throw switch may allow selection of the short circuit path 764.

[0092] In effect, selected subsets of the plurality of capacitors 760 form the capacitance C_{tuning} discussed previously. Since there is no requirement for the constituent capacitors of

the plurality of capacitors to be identical, C_{tuning} can be tailored as needed for a given application. However, the simple example of n identical fixed capacitors 762 each with capacitance C_0 is useful for illustrating the functionality of the tuning circuit 701. Then $C_{tuning} = nC_0$. In the absence of other capacitive components the variable capacitance of the tuning circuit 701 would range from 0 to nC_0 in discrete C_0 steps.

[0093] However, if another capacitive component is also included in series (e.g. a capacitive pre-coat layer) then the total capacitance $C_n = (1/C_{fixed} + 1/nC_0)^{-1}$. Although n cannot be zero in this equation, it is noted that the $n = 0$ case (where a short circuit path is selected) would make $C = C_{fixed}$ as previously discussed. In the specific example where C_{fixed} = 100 nF and C_0 = 5 nF, $C_{n=1, 2, 3 \ldots}$ = { 4.8 nF, 9.1 nF, 13 nF, ... }. Of course, fixed capacitors are available with capacitance values both lower and higher than 5 nF.

[0094] The increase in total capacitance for each added capacitor decreases as n increases. For example, C_{20} = 50 nF, but C_{30} = 60 nF. Notably, in the absence of C_{fixed}, C_{20} = 100 nF and C_{30} = 150 nF. Therefore, the combination of a capacitive pre-coat layer and a tuning circuit may be desirable when a high maximum capacitance is desirable (e.g. 100 nF), but there is not sufficient space for a large number capacitors in a tuning circuit. The relatively small number of capacitors in the tuning circuit would then permit granular capacitance selection in the lower range such as about 5 nF (n = 1) to about 33 nF (n = 10), for example.

[0095] FIG. 8 illustrates a schematic diagram of an example tuning circuit comprising a single pole switch and a plurality of variable capacitors in accordance with an embodiment of the invention. The tuning circuit of FIG. 8 may be a specific implementation of other tuning circuits described herein such as the tuning circuit of FIG. 7, for example. Similarly labeled elements may be as previously described.

[0096] Referring to FIG. 8, a tuning circuit 801 includes a first tuning input/output 857, a second tuning input/output 859, and a plurality of capacitors 860 which may include variable capacitors 861 arranged in banks of capacitors 863 as shown. In various embodiments, the variable capacitors 861 are high reliability capacitors. In some embodiments, some or all of the variable capacitors 861 are vacuum capacitors. In some embodiments, some or all of the variable capacitors 861 are ceramic capacitors. The tuning circuit 801 further includes a first single pole switch 871 and may also include an optional second single pole switch 872. An optional short circuit path 864 may also be included.

[0097] The tuning circuit 801 differs from the tuning circuit 701 in that variable capacitors 861 are utilized rather than fixed capacitors. This may have the additional advantage of allowing smooth capacitance transitions over the available range of the variable

capacitance. However, the variable capacitors may have lower capacitance than fixed capacitors and may also be larger and more expensive.

[0098] FIG. 9 illustrates a schematic diagram of an example tuning circuit comprising a single pole switch and a plurality of capacitors including fixed capacitors and variable capacitors in accordance with an embodiment of the invention. The tuning circuit of FIG. 9 may be a specific implementation of other tuning circuits described herein such as the tuning circuit of FIG. 7, for example. Similarly labeled elements may be as previously described.

[0099] Referring to FIG. 9, a tuning circuit 901 includes a first tuning input/output 957, a second tuning input/output 959, and a plurality of capacitors 960 which may include variable capacitors 961 as well as fixed capacitors 962 arranged in banks of capacitors 963 as shown. The tuning circuit 901 further includes a first single pole switch 971 and may also include an optional second single pole switch 972. An optional short circuit path 964 may also be included.

[0100] The tuning circuit 901 differs from the tuning circuit 701 and the tuning circuit 801 in that both variable capacitors 961 and fixed capacitors 962 are utilized. This may beneficially allow expanded range of the variable capacitance while also improving the fine control of the capacitance.

[0101] FIG. 10 illustrates a schematic diagram of an example tuning circuit comprising a single pole switch and a plurality of capacitors in accordance with an embodiment of the invention. The tuning circuit of FIG. 10 may be a specific implementation of other tuning circuits described herein such as the tuning circuit of FIG. 7, for example. Similarly labeled elements may be as previously described.

[0102] Referring to FIG. 10, a tuning circuit 1001 includes a first tuning input/output 1057, a second tuning input/output 1059, and a plurality of capacitors 1060 which may include fixed capacitors 1062 arranged in banks of capacitors 1063 as shown. The tuning circuit 1001 further includes a first single pole switch 1071 and may also include an optional second single pole switch 1072.

[0103] The tuning circuit 1001 is a specific implementation of the tuning circuit 701 where a short circuit path is omitted. This configuration may be useful, for example, when the capacitive pre-coat layer is omitted. As previously discussed, variable capacitors may also be utilized instead of or in addition to the fixed capacitors 1062.

[0104] FIG. 11 illustrates a schematic diagram of an example plasma processing apparatus comprising a capacitive pre-coat layer covering an upper electrode, and a tuning circuit coupled to the upper electrode in accordance with an embodiment of the invention. The plasma processing apparatus of FIG. 11 may be a specific implementation of other

plasma processing apparatuses described herein such as the plasma processing apparatus of FIG. 3, for example. Similarly labeled elements may be as previously described.

[0105] Referring to FIG. 11, a plasma processing apparatus 1100 includes a substrate holder 1104 configured to support a substrate 1105 and disposed in an interior 1103 of a plasma processing chamber 1102. A source power supply 1107 that is configured to generate plasma 1106 is coupled to a source power coupling element 1151. A tuning circuit 1101 is coupled between a DC pulse generator 1108 and a DC coupling element 1153. A bias power supply 1109 is coupled to the DC pulse generator 1108. A reference potential node 1145 is coupled to the substrate holder 1104.

[0106] The plasma processing apparatus 1100 differs from the plasma processing apparatus illustrated in FIG. 3 in that the DC coupling element 1153 is implemented as an upper electrode at the top of the interior 1103 of the plasma processing chamber 1102. The voltage applied by the DC pulse generator 1108 to the DC coupling element 1153 may be positive (as opposed to negative) in order to create a potential gradient that accelerates positive ions towards the substrate 1105 which may be at or near the reference potential. A DC current path then exists from the bias power supply 1109 to the reference potential node 1145.

[0107] An optional capacitive pre-coat layer 1144 may be included on the DC coupling element 1153. Additionally, since the reference potential node 1145 is coupled to the substrate holder 1104 rather than a wall of the plasma processing chamber 1102, resistive components may be included between the substrate 1105 and the reference potential node 1145. For example, an optional resistive pre-coat layer (not shown) may be included on the surface of the substrate holder 1104. Alternatively or additionally, resistors may also be included to increase the resistance.

[0108] FIG. 12 illustrates an example method of plasma processing in accordance with an embodiment of the invention. The method of FIG. 12 may be combined with other methods and performed using the systems and apparatuses as described herein. For example, the method of FIG. 12 may be combined with any of the embodiments of FIGS. 1–11. Although shown in a logical order, the arrangement and numbering of the steps of FIG. 12 are not intended to be limited. The method steps of FIG. 12 may be performed in any suitable order or concurrently with one another as may be apparent to a person of skill in the art.

[0109] Referring to FIG. 12, a step 1201 of a method 1200 of plasma processing includes determining a capacitance value from a range of capacitance values according to a DC pulse frequency of a DC pulse train to be generated by a DC pulse generator of a plasma processing

apparatus. Step 1202 includes tuning an electrical characteristic by selecting the determined capacitance value using a tuning circuit coupled between a DC coupling element and the DC pulse generator, the tuning circuit comprising a variable capacitance tunable in the range of capacitance values.

[0110] Plasma is optionally generated in a plasma processing chamber of the plasma processing apparatus by applying source power to the plasma processing chamber in optional step 1203. Alternatively, the plasma may already be present in the plasma processing chamber. Step 1204 includes biasing the DC coupling element relative to a reference potential node by generating the DC pulse train at the DC pulse frequency using the DC pulse generator. The DC coupling element may be biased in an afterglow phase of the plasma (e.g. after removal of source power).

[0111] Example embodiments of the invention are summarized here. Other embodiments can also be understood from the entirety of the specification as well as the claims filed herein.

[0112] Example 1. A plasma processing apparatus including: a plasma processing chamber; a SP coupling element configured to generate plasma in an interior of the plasma processing chamber by coupling source power to the plasma processing chamber; a DC pulse generator configured to generate a DC pulse train at a DC pulse frequency; a substrate holder disposed in the interior of the plasma processing chamber; a DC coupling element coupled to the DC pulse generator; a DC current path including the DC coupling element, the plasma, and a reference potential node in a series configuration, the DC coupling element being configured to bias the substrate holder relative to the reference potential node using the DC pulse train; and a capacitive pre-coat layer disposed between the DC coupling element and the plasma, the capacitive pre-coat layer increasing the RC time constant of the DC current path according to the DC pulse frequency.

[0113] Example 2. The plasma processing apparatus of example 1, where the capacitive pre-coat layer increases the RC time constant to at least double the inverse of the DC pulse frequency.

[0114] Example 3. The plasma processing apparatus of one of examples 1 and 2, where the capacitance of the capacitive pre-coat layer is about 100 nF.

[0115] Example 4. The plasma processing apparatus of one of examples 1 to 3, where a thickness of the capacitive pre-coat layer is about 600 nm.

[0116] Example 5. The plasma processing apparatus of one of examples 1 to 4, where the capacitive pre-coat includes silicon, silica, or yttria.

[0117] Example 6. The plasma processing apparatus of one of examples 1 to 5, further including: a resistive pre-coat layer disposed on surfaces of the interior of the plasma processing chamber; where the reference potential node is coupled to the plasma processing chamber; where the resistive pre-coat layer is disposed between the plasma and the reference potential node; and where the resistive pre-coat layer further increases the RC time constant of the DC current path according to the DC pulse frequency.

[0118] Example 7. The plasma processing apparatus of example 6, where the resistance of the resistive pre-coat layer is about 1 kΩ.

[0119] Example 8. The plasma processing apparatus of one of examples 6 and 7, where a thickness of the resistive pre-coat layer is about 100 nm.

[0120] Example 9. The plasma processing apparatus of one of examples 6 to 8, where the resistive pre-coat layer includes amorphous carbon, graphitic carbon, a silicon-like material, or a silica-like material.

[0121] Example 10. The plasma processing apparatus of one of examples 1 to 9, further including: a tuning circuit coupled between the DC coupling element and the DC pulse generator, the tuning circuit including a variable capacitance.

[0122] Example 11. The plasma processing apparatus of one of examples 1 to 10, where the substrate holder is an electrostatic chuck (ESC).

[0123] Example 12. The plasma processing apparatus of one of examples 1 to 11, where the DC coupling element is disposed above the substrate holder; and the reference potential node is coupled to the substrate holder.

[0124] Example 13. A plasma processing apparatus including: a plasma processing chamber; a SP coupling element configured to generate plasma in an interior of the plasma processing chamber by coupling source power to the plasma processing chamber; a DC pulse generator configured to generate a DC pulse train including a DC pulse frequency; a substrate holder disposed in the interior of the plasma processing chamber; a DC coupling element coupled to the DC pulse generator; a DC current path including the DC coupling element, the plasma, and a reference potential node in a series configuration, the DC coupling element being configured to bias the substrate holder relative to the reference potential node using the DC pulse train; and a tuning circuit coupled between the DC coupling element and the DC pulse generator, the tuning circuit including a variable capacitance, the tuning circuit being configured to tune an RC time constant of the DC current path by varying the variable capacitance according to the DC pulse frequency.

[0125] Example 14. The plasma processing apparatus of example 13, where the tuning circuit includes a variable capacitor.

[0126] Example 15. The plasma processing apparatus of one of examples 13 and 14, where the tuning circuit includes: a plurality of capacitors; a first single pole switch including an input coupled to either the DC coupling element or the DC pulse generator, and a first output coupled to a first subset of the of plurality of capacitors.

[0127] Example 16. The plasma processing apparatus of example 15, where the first single pole switch is a mechanical switch.

[0128] Example 17. The plasma processing apparatus of example 16, where the first single pole switch is an electromechanical switch.

[0129] Example 18. The plasma processing apparatus of one of examples 15 to 17, where the tuning circuit further includes: a second single pole switch including an input coupled to the DC pulse generator and an output coupled to the first subset of the plurality of capacitors, where the first single pole switch is coupled to the DC coupling element.

[0130] Example 19. The plasma processing apparatus of one of examples 15 to 18, where the plurality of capacitors includes a plurality of banks of capacitors coupled in parallel with one another.

[0131] Example 20. The plasma processing apparatus of one of examples 15 to 19, where the first single pole switch is a multiple throw switch including a second output coupled to a second subset of the plurality of capacitors.

[0132] Example 21. The plasma processing apparatus of example 20, where the first single pole multiple throw switch is a rotary switch.

[0133] Example 22. The plasma processing apparatus of one of examples 20 and 21, where the capacitors of the first subset and the capacitors of the second subset are mutually exclusive.

[0134] Example 23. The plasma processing apparatus of one of examples 15 to 18, where: the first single pole switch is a single throw switch; and the tuning circuit further includes a second single pole single throw switch including an input coupled to the input of the first single pole single throw switch, and an output coupled to a second subset of the plurality of capacitors.

[0135] Example 24. The plasma processing apparatus of one of examples 15 to 23, where the plurality of capacitors includes a plurality of fixed capacitors.

[0136] Example 25. The plasma processing apparatus of example 24, where the plurality of capacitors further includes a variable capacitor.

[0137] Example 26. The plasma processing apparatus of one of examples 15 to 25, where the first single pole switch includes a second output coupled to either the DC pulse generator or the DC coupling element so that a short circuit path is formed between the DC coupling element and the DC pulse generator when the second output is selected.

[0138] Example 27. The plasma processing apparatus of one of examples 13 to 26, further including: a resistive pre-coat layer disposed on surfaces of the interior of the plasma processing chamber; where the reference potential node is coupled to the plasma processing chamber; where the resistive pre-coat layer is disposed between the plasma and the reference potential node; and where the resistive pre-coat layer further increases the RC time constant of the DC current path according to the DC pulse frequency.

[0139] Example 28. The plasma processing apparatus of example 27, further including: a capacitive pre-coat layer disposed between the DC coupling element and the plasma, the capacitive pre-coat layer increasing the RC time constant of the DC current path according to the DC pulse frequency.

[0140] Example 29. A method of tuning an electrical characteristic of a plasma processing chamber of a plasma processing apparatus, the method including: determining a capacitance value from a range of capacitance values according to a direct current (DC) pulse frequency of a DC pulse train to be generated by a DC pulse generator of the plasma processing apparatus; tuning the electrical characteristic by selecting the determined capacitance value using a tuning circuit coupled between a DC coupling element and the DC pulse generator, the tuning circuit including a variable capacitance tunable in the range of capacitance values; and biasing the DC coupling element relative to a reference potential node by generating the DC pulse train at the DC pulse frequency using the DC pulse generator.

[0141] Example 30. The method of example 29, further including: generating plasma in the plasma processing chamber by applying source power to the plasma processing chamber prior to biasing the DC coupling element; and where biasing the DC coupling element includes biasing the DC coupling element in an afterglow of the plasma after removal of the source power.

[0142] Example 31. The method of one of examples 29 and 30, where biasing the DC coupling element includes negatively biasing a substrate holder in the plasma processing chamber relative to the reference potential node by generating the DC pulse train at the DC pulse frequency using the DC pulse generator.

[0143] Example 32. The method of one of examples 29 to 31, where the electrical characteristic includes an RC time constant of a DC current path including the DC coupling element, a plasma in the plasma processing chamber, and the reference potential node.

[0144] Example 33. The method of example 32, where the RC time constant is at least double the inverse of the DC pulse frequency.

[0145] Example 34. The method of example 33, where the DC pulse frequency is less than about 400 kHz.

[0146] Example 35. The method of example 34, where the DC pulse frequency is less than about 20 kHz.

[0147] While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. It is therefore intended that the appended claims encompass any such modifications or embodiments.

WHAT IS CLAIMED IS:

1. A plasma processing apparatus comprising:

a plasma processing chamber;

a source power (SP) coupling element configured to generate plasma in an interior of the plasma processing chamber by coupling source power to the plasma processing chamber;

a direct current (DC) pulse generator configured to generate a DC pulse train at a DC pulse frequency;

a substrate holder disposed in the interior of the plasma processing chamber;

a DC coupling element coupled to the DC pulse generator;

a DC current path comprising the DC coupling element, the plasma, and a reference potential node in a series configuration, the DC coupling element being configured to bias the substrate holder relative to the reference potential node using the DC pulse train; and

a capacitive pre-coat layer disposed between the DC coupling element and the plasma, the capacitive pre-coat layer increasing the RC time constant of the DC current path according to the DC pulse frequency.

2. The plasma processing apparatus of claim 1, further comprising:

a resistive pre-coat layer disposed on surfaces of the interior of the plasma processing chamber;

wherein the reference potential node is coupled to the plasma processing chamber;

wherein the resistive pre-coat layer is disposed between the plasma and the reference potential node; and

wherein the resistive pre-coat layer further increases the RC time constant of the DC current path according to the DC pulse frequency.

3. The plasma processing apparatus of claim 1, further comprising:

a tuning circuit coupled between the DC coupling element and the DC pulse generator, the tuning circuit comprising a variable capacitance.

4. The plasma processing apparatus of claim 1, wherein:

the DC coupling element is disposed above the substrate holder; and

the reference potential node is coupled to the substrate holder.

5. A plasma processing apparatus comprising:

a plasma processing chamber;

a source power (SP) coupling element configured to generate plasma in an interior of the plasma processing chamber by coupling source power to the plasma processing chamber;

a direct current (DC) pulse generator configured to generate a DC pulse train

comprising a DC pulse frequency;

a substrate holder disposed in the interior of the plasma processing chamber;

a DC coupling element coupled to the DC pulse generator;

a DC current path comprising the DC coupling element, the plasma, and a reference potential node in a series configuration, the DC coupling element being configured to bias the substrate holder relative to the reference potential node using the DC pulse train; and

a tuning circuit coupled between the DC coupling element and the DC pulse generator, the tuning circuit comprising a variable capacitance, the tuning circuit being configured to tune an RC time constant of the DC current path by varying the variable capacitance according to the DC pulse frequency.

6. The plasma processing apparatus of claim 5, wherein the tuning circuit comprises:

a plurality of capacitors;

a first single pole switch comprising an input coupled to either the DC coupling element or the DC pulse generator, and a first output coupled to a first subset of the of plurality of capacitors.

7. The plasma processing apparatus of claim 6, wherein the tuning circuit further comprises:

a second single pole switch comprising an input coupled to the DC pulse generator and an output coupled to the first subset of the plurality of capacitors, wherein the first single pole switch is coupled to the DC coupling element.

8. The plasma processing apparatus of claim 6, wherein the plurality of capacitors comprises a plurality of banks of capacitors coupled in parallel with one another.

9. The plasma processing apparatus of claim 6, wherein the first single pole switch is a multiple throw switch comprising a second output coupled to a second subset of the plurality of capacitors.

10. The plasma processing apparatus of claim 6, wherein:

the first single pole switch is a single throw switch; and

the tuning circuit further comprises a second single pole single throw switch comprising an input coupled to the input of the first single pole single throw switch, and an output coupled to a second subset of the plurality of capacitors.

11. The plasma processing apparatus of claim 6, wherein the plurality of capacitors comprises a plurality of fixed capacitors.

12. The plasma processing apparatus of claim 6, wherein the first single pole switch comprises a second output coupled to either the DC pulse generator or the DC coupling element so that a short circuit path is formed between the DC coupling element and the DC pulse generator when the second output is selected.

13. The plasma processing apparatus of claim 5, further comprising:

a resistive pre-coat layer disposed on surfaces of the interior of the plasma processing chamber;

wherein the reference potential node is coupled to the plasma processing chamber;

wherein the resistive pre-coat layer is disposed between the plasma and the reference potential node; and

wherein the resistive pre-coat layer further increases the RC time constant of the DC current path according to the DC pulse frequency.

14. The plasma processing apparatus of claim 13, further comprising:

a capacitive pre-coat layer disposed between the DC coupling element and the plasma, the capacitive pre-coat layer increasing the RC time constant of the DC current path according to the DC pulse frequency.

15. A method of tuning an electrical characteristic of a plasma processing chamber of a plasma processing apparatus, the method comprising:

determining a capacitance value from a range of capacitance values according to a direct current (DC) pulse frequency of a DC pulse train to be generated by a DC pulse generator of the plasma processing apparatus;

tuning the electrical characteristic by selecting the determined capacitance value using a tuning circuit coupled between a DC coupling element and the DC pulse generator, the tuning circuit comprising a variable capacitance tunable in the range of capacitance values; and

biasing the DC coupling element relative to a reference potential node by generating the DC pulse train at the DC pulse frequency using the DC pulse generator.

16. The method of claim 15, further comprising:

generating plasma in the plasma processing chamber by applying source power to the plasma processing chamber prior to biasing the DC coupling element; and

wherein biasing the DC coupling element comprises biasing the DC coupling element in an afterglow of the plasma after removal of the source power.

17. The method of claim 15, wherein biasing the DC coupling element comprises negatively biasing a substrate holder in the plasma processing chamber relative to the

reference potential node by generating the DC pulse train at the DC pulse frequency using the DC pulse generator.

18. The method of claim 15, wherein the electrical characteristic comprises an RC time constant of a DC current path comprising the DC coupling element, a plasma in the plasma processing chamber, and the reference potential node.

19. The method of claim 18, wherein the RC time constant is at least double the inverse of the DC pulse frequency.

20. The method of claim 19, wherein the DC pulse frequency is less than about 400 kHz.