PACKAGING STRUCTURAL MEMBER

BACKGROUND

[0001] In semiconductor fabrication, a plurality of silicon dies are typically formed in parallel on a common substrate and further processed to encapsulate the dies in mold compound. After processing of the die-substrate assembly is completed, it is diced to separate or singulate the assembly into individual units.

[0002] One challenge in providing the encapsulation is that warpage may occur due to a mismatch in the Coefficient of Thermal Expansion (CTE) of the mold compound and the silicon die. This problem becomes aggravated when the encapsulation is carried out on an array of silicon dies mounted onto a common substrate such as in a wafer format, and even more so when the thickness of the silicon dies and the substrate decreases. Furthermore, when mounted onto a common substrate, the silicon dies may shift out of its designated location during molding. Additionally, another challenge faced by this form of assembly is optimising the number of dies that can be mounted onto the common substrate so as to maximise space savings.

[0003] Based on the foregoing discussion, the packages and/or package techniques are desirable to address one or more of the above disadvantages.

SUMMARY

[0004] A method of assembling devices is disclosed. One embodiment employs the use of a structural member which is mated to a first surface of a temporary carrier substrate with an adhesive. The structural member includes a plurality of die package regions. A die package region has a die attach region surrounded by a peripheral region. Dies are attached to the die attach regions of the structural member. Through-vias are disposed in the package regions of the structural member. The through-vias comprise a conductive material and are electrically coupled to bond pads of the dies.

[0005] In another embodiment a semiconductor package is disclosed. The package includes a structural member having first and second major surfaces. The structural member includes a

die attach region surrounded by a peripheral region. The die attach region accommodates a die to be packaged. At least one through-via is disposed in the structural member. The through-vias extend through the first and second surfaces of the structural member.

[0006] In yet another embodiment, a method of assembling a device is disclosed. One embodiment employs the use of a structural member which is mated to a first surface of a temporary carrier substrate with an adhesive. The structural member includes a die package region. The die package region has a die attach region surrounded by a peripheral region. A die is attached to the die attach region of the structural member. Through-vias are disposed in the package region of the structural member. The through-vias comprise a conductive material and are electrically coupled to bond pads of the die.

[0007] A die attach region can, for example, comprise an opening extending through the surfaces of the structural member for accommodating a die therein. The structural member can reduce warpage that can occur during curing of the mold compound used in encapsulating the die.

[0008] In other embodiments, the die attach region does not have an opening. In such case, the top surfaces of the die attach and peripheral regions may be coplanar. The die is attached to the structural member in the die attach region. Through-vias are disposed in the die attach region, electrically coupling bond pads of the die. The structural member can serve as an interposer which balances CTE of the components of the package.

[0009] Furthermore, other aspects include RDL layers on top and bottom of the package. The RDL layers provide contact pads on top and bottom of the surfaces. The contact pads on the top and bottom surfaces are coupled by the through-vias, which facilitates stacking of the packages.

[0010] These and other objects, along with advantages and features of the present invention herein disclosed, will become apparent through reference to the following description and the accompanying drawings. Furthermore, it is to be understood that the features of the various

embodiments described herein are not mutually exclusive and can exist in various combinations and permutations.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] In the drawings, like reference characters generally refer to the same parts throughout the different views. Also, the drawings are not necessarily to scale, emphasis instead generally being placed upon illustrating the principles of the invention. In the following description, various embodiments of the present invention are described with reference to the following drawings, in which:

[0012] Figs. 1a-1b show the top and side views of an embodiment of a structural member;

[0013] Figs. 1c-1d show the top and side views of another embodiment of a structural member;

[0014] Figs. 2a-2b show embodiments of enlarged portions of a structural member;

[0015] Figs. 3a-3b show other embodiments of enlarged portions of a structural member;

[0016] Figs. 4a-4c show an embodiment of a process employing a structural member;

[0017] Figs. 5a-5b to Figs. 7a-7b show other processes employing a structural member;

[0018] Figs. 8a-8b show embodiments of stack packages;

[0019] Fig. 9 shows another embodiment of a stack package; and

[0020] Figs 10a-10c show embodiments of stack packages.

DETAILED DESCRIPTION

[0021] Embodiments generally relate to semiconductor devices or integrated circuits (ICs), which are widely used in applications, such as micro-controllers, wired and wireless data networking, consumer electronics etc. In particular, embodiments relate to a structural member used in packaging the ICs.

[0022] Figs. 1a and 1b show simplified top and side views of an embodiment of a structural member 200. Figs. 1c and 1d show top and side views of another embodiment of a structural member 200. Referring to the Figs. 1a-1d, the structural member 200 facilitates packaging of a

plurality of dies in parallel onto a common substrate or carrier. The structural member 200 comprises a frame 210. As shown in Fig. 1a, the frame 210 is of a circular shape, for example, a wafer format. Other geometric shapes may also be useful. For example, as shown in Fig. 1c, the frame 210 may have a square or rectangular shape. Providing a frame in a strip format or other formats is also useful.

[0023] Within the frame is a plurality of package regions 230. A package region, in one embodiment, comprises a die attach regions 231 surrounded by a peripheral region 232. A die attach region 231 accommodates a die. The die attach region 231 comprises, for example, an opening (see, for example, element 350 in Figs. 2a and 2b). The opening, in one embodiment, extends through the top and bottom surfaces of the frame. In one embodiment, the dies which are to be packaged are disposed in the openings. The size and shape of the opening should accommodate the dies. For example, the openings comprise a rectangular shape and have a size sufficient to fit the dies. Providing non-rectangular shaped openings may also be useful. Preferably, the structural member comprises openings which are of the same size and/or same shape for packaging the same type of dies. Alternatively, the structural member may have openings of different sizes and/or shapes for packaging different types of die sizes and/or shapes.

[0024] In yet other embodiments, the die attach region 231 is devoid of an opening. The structural member, for example, may comprise a planar member. For such applications, the die is attached to the structural member 200 in the die attach region. The structural member, for example, serves as an interposer which is sandwiched between a die and a substrate. An exemplary application of the structural member 200 as an interposer is shown in Fig. 10a.

[0025] In a preferred embodiment, the package regions 230 are arranged in rows and columns to form an array. The rows and columns need not have the same number of die attach regions. The number of package regions per row and/or column may depend on, for example, the size of the package regions, size of the frame, shape of the frame or a combination thereof.

In the case of a circular frame, for example, the number of package regions of columns and rows toward the edge of the frame may be less than those towards the center of the frame.

[0026] The package regions are separated by rails 220 in first and second directions. For example, the openings are separated by rails 220 in the first and second directions. The first and second directions are generally orthogonal to each other. As illustrated, the x and y directions are orthogonal to each other. The rails 220, for example, are integral to the frame 210. In one embodiment, the peripheral regions of the package regions can be disposed in the rails. It is understood that the rails need not be physically distinct from the die attach regions to form a grid. For example, the rails and die attach regions can be integrated to form a planar structural member, such as in the case where the die attach regions are devoid of openings. Alignment lines (not shown) may be provided on the rails. The alignment lines are in the first and second directions. For example, the alignment lines serve as saw lines or saw streets for singulating the packaged dies into individual devices.

[0027] Various types of materials may be employed to form the frame 210 and the rails 220. In one embodiment, the frame 210 comprises substrate core materials, including ceramic based materials such as alumina. Other types of materials, such as mold compounds or organic materials, including polyamide, Bismaleimide Triazine (BT) resin or FR-4 or FR-5 materials, may also be useful. The material of the structural member, for example, can be selected to balance CTE of the components of the package.

[0028] The frame may be formed using various techniques. For example, the frame may be formed by compression molding, lamination or stencil printing. Other techniques may also be employed to form the frame. The technique, for example, may depend on the type of materials used to form the frame.

[0029] The frame comprises a thickness T. In one embodiment, T is equal to or greater than a thickness of the dies to be encapsulated. In another embodiment, T is less than the thickness of

the dies to be encapsulated. By providing die attach regions with openings in which dies are disposed, shifting of the dies during encapsulation is reduced or prevented.

[0030] Figs. 2a-2b show enlarged portions 340 of different embodiments of a structural member 200. The enlarged portions 340 illustrate two adjacent package regions 230 of the structural member 200. A package region 230 comprises a die attach region 231 surrounded by a peripheral region 232. As illustrated, the die attach region 231 comprises an opening 350. The opening, for example, extends through the surfaces of the structural member. The package region 230, in one embodiment, comprises at least one through-via 360. Generally, a plurality of through-vias are disposed in the package region. In one embodiment, the through-vias are disposed in the peripheral region 232 of the package region. The through-vias 360 extend through the top and bottom surfaces of the frame 210. The through-vias 360 can be distributed in any arrangement in the peripheral region 232. For example, the through-vias 360 can be arranged in a line in the peripheral region surrounding the opening, as shown. Other arrangements of through-vias are also useful.

[0031] The through-vias 360 can be formed by various techniques. Such techniques can include laser drilling or Deep Reactive Ion Etching (DRIE). Other techniques are also useful. In one embodiment, the vias 360 are filled with a conductive material 365. For example, the vias are filled with copper or copper alloy. Filling the vias with other types of materials is also useful. In one embodiment, the vias are filled by electroplating. The vias can also be filled using other filling techniques. As shown in Fig. 2a, the vias are completely filled with a conductive material 365. Alternatively, as shown in Fig. 2b, the vias are lined with a conductive material 365.

[0032] Figs. 3a-3b show enlarged portions 440 of other embodiments of a structural member 200. The enlarged portions 440 illustrate two adjacent package regions 230 of the structural member 200. A package region, for example, comprises a die attach region 231 surrounded by a

peripheral region 232. In one embodiment, the die attach regions comprise no openings. For example, the structural member comprises a planar member.

[0033] A package region 230, in one embodiment, comprises at least one through-via 360 therein. Generally, a plurality of through-vias 360 are provided in the package region 230. The through-vias 360 can be distributed in the package region 230 in any configuration. For example, the through-vias 360 can be distributed uniformly throughout the package region (e.g., both die attach region 231 and peripheral region 232), as shown in Fig. 3a or be arranged in the peripheral region 232, as shown in Fig. 3b. Distributing the through-vias 360 in other configurations is also useful.

[0034] The through-vias may extend through the top and bottom surfaces of the frame 210. The through-vias 360 may be formed by various techniques. Such techniques may include laser drilling or Deep Reactive Ion Etching (DRIE). Other techniques are also useful.

[0035] In one embodiment, the vias 360 are filled with a conductive material 365. For example, the vias 360 are filled with copper or copper alloy. Filling the vias with other types of materials is also useful. In one embodiment, the vias 360 are filled by electroplating. The vias can also be filled using other filling techniques. As shown in Fig. 3a, the vias are completely filled with a conductive material 365. Alternatively, as shown in Fig. 3b, the vias 360 are lined with a conductive material 365.

[0036] Figs. 4a-4b illustrate cross-sectional views of an embodiment of a process for assembling a semiconductor package 500. Fig. 4c shows a plan view of the process corresponding to Fig. 4a. For simplification, the Figures show a portion 540 depicting two adjacent package regions 230.

[0037] Referring to Fig. 4a and Fig. 4c, a temporary support carrier 570 is provided. The temporary support carrier 570, for example, provides a common carrier to which a plurality of dies 510 are mounted for assembly. The temporary support carrier 570 may be formed from various types of materials. For example, the temporary support carrier 570 comprises copper,

glass, silicon, quartz, sapphire or any other material that is sufficiently rigid to withstand further processing steps. Other types of materials which can provide mechanical support to the dies are also useful.

[0038] The top surface of the temporary support carrier 570 is coated with an adhesive 572. The adhesive can be any temporary adhesive which can lose its adhesive strength when subjected to a treatment. In one embodiment, the adhesive loses its adhesive strength when heated to a threshold temperature. Mated to the top surface of the temporary support carrier 570 is a structural member 200. In one embodiment, the structural member 200 is temporarily mated to the top surface with the adhesive. Once the adhesive is treated to lose its adhesive strength, the support carrier can be separated or dislodged from the structural member.

[0039] The structural member 200 comprises a plurality of package regions 230. A package region includes a die attach region 231. The structural member facilitates assembly of dies in, for example, a wafer format. The structural member may also be configured to facilitate assembling the dies in other formats. In one embodiment, the die attach regions comprise openings 350. Through-vias 360 filled with a conductive material 365, such as copper or copper alloy, are provided. In other embodiments, the sidewalls of the through-vias are coated with conductive material 365. The through-vias, for example, are disposed in the rail portions 220 of the structural member 200 (e.g., peripheral regions 232) peripheral to the opening 350. In one embodiment, the structural member is prefabricated with openings and through-vias filled or lined with a conductive material prior to mating to the substrate. In other embodiments, the through-vias may be formed and filled after being mated to the substrate. The through-vias may be formed before or after encapsulation.

[0040] In one embodiment, dies 510 are disposed in the openings 350 of the structural member 200. The dies 510 are temporarily attached to the support carrier 570 by the adhesive 572. As shown, an active surface 511 of the die with die bond pads 516 disposed thereon is mated to the support carrier 570. The thickness T of the structural member, in one embodiment,

is the same or substantially the same as the height of the die. This results in top surfaces of the structural member and die being about coplanar.

[0041] Since the dies are smaller than the opening, gaps 525 exist between the dies and opening sidewalls. After the dies are mated to the support carrier 570 surface, the dies 510 are encapsulated by filling the gaps with a mold compound 535. In one embodiment, the top surface of the mold compound 535 is flush with the top surfaces of the die 510 and structural member 200. The structural member, for example, acts as a stencil for filling the gaps. The structural member 200 may also reduce shifting of the dies 510 during encapsulation. After encapsulation, the mold compound is cured. Curing, for example, comprises exposing the die assembly to heat.

[0042] Referring to Fig. 4c, a top redistribution layer (RDL) 580 is formed on the assembly. For example, the top RDL 580 is formed on the top surface of the frame 210 and inactive surface of the die 510. The top RDL 580, for example, comprises conductive lines. RDL contact pads 585 are formed along the top RDL 580. The conductive lines couple the RDL contact pads 585 to the through-vias 360 at the periphery of the opening 350. The pattern of the RDL contact pads 585 corresponds to, for example, the pattern of contact pads of another package or chip to be stacked on the top RDL. The RDL can be formed by various techniques. For example, the RDL can be formed by electroplating. Other techniques for forming the RDL are also useful.

[0043] In one embodiment, the temporary support carrier 570 is detached from the assembly after the top RDL is formed. Detachment can be achieved by, for example, heating the adhesive until it loses its adhesive strength, enabling the support carrier 570 to be dislodged. Removing the support carrier 570 exposes the active surface 511 of the dies 510. In one embodiment, a bottom RDL 581 is formed on the bottom surface of the assembly. The bottom RDL contacts the bottom surface of the structural member 200 and active surface 511 of the die 510. The bottom RDL 581 couples the die bond pads 516 to the through-vias 360, resulting in the die pads being coupled to the top RDL 580 and top RDL contact pads 585. The top and bottom RDLs facilitate stacking of dies or other packages to reduce overall footprint of the device.

[0044] A singulation process is performed after assembly is completed to separate the packages into individual packages. In one embodiment, the singulation process comprises sawing the frame along saw lines or saw streets to separate the die attach regions into individual packages.

[0045] Advantageously, the structural member 200 provides structural integrity or mechanical support to the array of dies in wafer format or other formats to prevent warpage from occurring during the assembly process and in particular during the encapsulation and curing process. The structural member 200 may also prevent the dies 510 from shifting out of its designated locations during encapsulation. The structural member 200 with the through-vias 360 is incorporated into the final package and can act as a pathway to connect the dies 510, through the bottom RDL 581, the through-vias 360, and the top RDL 580, to the top RDL contact pads 585. This can then facilitate stacking of further packages or dies onto the package.

[0046] Figs. 5a-5b show cross-sectional views of another embodiment of a process 600 for assembling a semiconductor package. The process is similar to that described in Figs. 4a-4b. The difference is that the frame 210 comprises a thickness T which is greater than the height of the dies 510. In one embodiment, the mold compound 535 filling the gaps 525 also covers the inactive surface 512 of the dies 510 such that the top surface of the mold compound 535 is about coplanar with the top surface of the frame 210. After encapsulation, the process continues as described. For example, the process continues by forming a top RDL layer 580, detaching the substrate 570, forming bottom RDL layer 581 and singulating the assembly.

[0047] As described, the mold compound is flush with the top surface of the frame. In alternative embodiments, the mold compound may cover both the frame and die. For applications in which the mold compound covers the frame, the through-vias are preferably formed after encapsulation. For example, through-vias are formed through the mold compound and frame.

[0048] Figs. 6a-6b and Figs. 7a-7b show cross-sectional views of other processes 700 and 800 for assembling a semiconductor package. The processes are similar to that described in Figs. 4a-4b. The difference is that the frame 210 comprises a thickness T which is less than the height of the dies 510. In one embodiment, the mold compound 535 filling the gaps 525 also covers the frame 210 such that the top surface of the mode compound is about coplanar with the inactive or top surface of the dies 510, as shown in Figs. 6a-6b. Alternatively, the mold compound 535 covers both the frame 210 and the dies 510, as shown in Figs. 7a-7b.

[0049] For applications in which the mold compound covers the frame, the through-vias 360 are preferably formed after encapsulation. For example, through-vias are formed through the mold compound and frame.

[0050] After encapsulation, the process continues as described. For example, the process continues by forming a top RDL layer 580, detaching the substrate 570, forming bottom RDL layer 581 and singulating the assembly.

[0051] In yet other embodiments, the structural member comprises a plurality of die attach regions 230 without openings. For example, the structural member 200 comprises a flat member. Through-vias 360 may be provided in the die attach region 230 to electrically couple the die 510 to a substrate.

[0052] In applications involving die attach regions without openings, the structural member 200 may serve as an interposer between the die and substrate to balance CTE mismatch between the components. The structural member 200 may also be used as a distribution pathway to couple die bonds pads of a certain pitch to substrate contact pads of a different or same pitch.

[0053] Figs. 8a-8b show embodiments of stack packages 900. In one embodiment, a stack package comprises a plurality of die packages $900_{1\text{-}N}$ configured in a stack. As shown, the stack package comprises a first package 900_1 with a second package 900_N (where N = 2) disposed thereabove. The stack package may comprise packages formed by any of the processes described above. For example, the packages includes a structural member 200 with mold

compound 535 filling at least gaps in the die attach region with a die 510. The packages may include top and bottom RDL layers 580 and 581 with through-vias 360.

[0054] In one embodiment, the packages comprise a structural member having the same height as the die. For example, the fill material has a top surface which is flush or coplanar with the top surfaces of the structural member and die. The structural member and the mold compound, for example, comprise different materials, as shown in Fig. 8a. Alternatively, the structural member and the mold compound comprise the same material, as shown in Fig. 8b. As illustrated, the packages of the stack are of the same type. In other embodiment, the packages of the stack may be different types of packages. For example, the die packages can comprise a combination of packages as described above, such as having structural members with different heights.

[0055] Fig. 9 shows another embodiment of a stack package 1000. As shown, the package comprises a first package 900. The first package can be a package formed by any of the processes described above. Package contacts 908 are provided on the bottom RDL of the first package. The package contacts, for example, are formed on contact pads of the bottom RDL. The package contacts may be configured in a ball grid array. Other package contact configurations may also be useful. Alternatively the first package can be a package stack, as described in Figs. 8a-8b. For example, the first package can be a package stack comprising N packages. In one embodiment, a device 902 which is disposed over the first package comprises a flip chip package. The flip chip includes chip bumps 909 on its active surface. The chip bumps may be configured in a ball grid array. Other configurations of chip bumps may also be useful. The pattern of the top RDL pads of the first package corresponds to the pattern of the chip bumps of the device.

[0056] The chip bumps 909 of the second package are coupled to the top RDL 580 of the first package. Alternatively, instead of a flip chip, the second package can be another package to form a Package-On-Package structure.

[0057] Referring to Figs. 8-9, it can be appreciated that the structural member 200 provides an access route coupling the die in the first package to a second package or die stacked above. In Fig. 8, the die in the first package 900_1 communicates with the die in the second package 900_N through the bottom RDL 581 of the first package, the through-vias 360 of the first package, the top RDL 580 of the first package and the bottom RDL 581 of the second package which is coupled to the die in the second package. Likewise in Fig. 10, the structural member 200 provides a similar mode of access from the die in the first package to the device or flip chip stacked thereon.

[0058] Figs. 10a-10c illustrate other embodiments of a semiconductor package 1100. Referring to Fig. 10a, the package comprises a substrate 874. The substrate 874 can for example be a Bismaleimide Triazine (BT) substrate. The substrate 874 includes top and bottom surfaces. The bottom surface is provided with package contacts 878. The package contacts, for example, are configured in a ball grid array. Other configurations of the package contacts may also be useful. The top surface, for example, includes substrate pads which are coupled to the package contacts by, for example, internal conductive traces.

[0059] A chip package 800 is mounted on the substrate 874. The chip package, in one embodiment, comprises a flip chip with chip bumps 808 on its active surface. The chip bumps are electrically coupled to the package contacts. In other embodiment, the chip package may comprise any of the packages as described in Figs. 4a-4b to 7a-7b.

[0060] In accordance with one embodiment, a structural member 200 is disposed between the chip package 800 and substrate 874. The structural member 200 comprises top and bottom RDLs. The top RDL comprises top RDL contact pads. The pattern of the top RDL contact pads corresponds to, for example, the chip bumps of the chip package. The bottom RDL comprises bottom RDL contact bumps 809. The pattern of the bottom RDL contact bumps, for example, corresponds to the substrate pads. The top and bottom RDL contact pads are coupled by the through-vias 360.

[0061] The chip package is mounted onto the top surface of the structural member. An underfill 833 may be provided between the chip bumps and top RDL. The bottom of the structural member is coupled to the top surface of the substrate. By disposing the structural member between the substrate and chip package, it acts as an interposer. The interposer provides electrical connection between the substrate and the chip package. In one embodiment, the structural member and chip package can be assembled in parallel, as previously described.

[0062] In one embodiment, the material of the structural member is appropriately selected to balance the CTE mismatch between the chip package, the filled through-vias and the substrate. The materials of the structural member can be selected from, for example, substrate core materials, mold compounds, organic materials or mixtures thereof. Other types of materials may also be useful.

[0063] The semiconductor package 1100, for example can be encapsulated by a mold compound 843, as shown in Fig. 10b. In other embodiments, the semiconductor package 1100 may be provided with underfill 834 between the interposer and substrate, as shown in Fig. 10c.

[0064] As described, one embodiment of the structural member may be made from mold compound material. One advantage of using mold compound as the structural member material is the flexibility in designing the properties of the mold compound. When designed and selected with the appropriate CTE and mechanical properties, the mold compound structural member improves thermal cycle reliability.

[0065] The invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. The foregoing embodiments, therefore, are to be considered in all respects illustrative rather than limiting the invention described herein. Scope of the invention is thus indicated by the appended claims, rather than by the foregoing description, and all changes that come within the meaning and range of equivalency of the claims are intended to be embraced therein.

What is claimed is:

CLAIMS

1. A semiconductor package comprising:

a structural member having first and second major surfaces, the structural member includes

a die attach region defined in the structural member, the die attach region accommodates a die for packaging and includes an opening passing through the major surfaces,

a peripheral region surrounding the die attach region,

at least one through-via disposed in the structural member, the through-via extending through the first and second surfaces of the structural member; and

a die being disposed in the opening, the die is smaller than the opening and gaps exist between the die and sidewalls of the opening, and the gaps are filled with a mold compound to encapsulate the die,

wherein a thickness of the structural member is less than a thickness of the die.

2. The semiconductor package of claim 1 comprises:

a top RDL layer on a top surface of the encapsulated die; and

a bottom RDL layer on a bottom surface of the encapsulated die, wherein the RDL layers and the at least one through-via facilitates stacking of packages.

3. The semiconductor package of claim 1 wherein the mold compound covers the first major surface of the structural member.

4. The semiconductor package of claim 3 wherein the at least one through-via extends through the mold compound and the first and second major surfaces of the structural member.

5. The semiconductor package of claim 4 wherein the structural member and the mold compound are separate components and comprise the same material.

6. The semiconductor package of claim 5 wherein the die includes first and second die surfaces, wherein the first die surface is an active surface and the first die surface is coplanar with a first surface of the mold compound.

7. The semiconductor package of claim 1 wherein the structural member and the mold compound are separate components and comprise the same material.

8. The semiconductor package of claim 6 wherein the second die surface is an inactive surface and the second die surface is coplanar with a second surface of the mold compound and the inactive surface of the die is exposed.

9. The semiconductor package of claim 1 wherein the mold compound covers the first major surface of the structural member and the die.

10. The semiconductor package of claim 1 wherein the structural member facilitates assembling devices in a wafer format.

11. The semiconductor package of claim 10 wherein the structural member and the mold compound are separate components and comprise the same material.

12. The semiconductor package of claim 11 wherein the mold compound covers the first major surface of the structural member.

13. The semiconductor package of claim 12 wherein the at least one through-via extends through the mold compound and the first and second major surfaces of the structural member.

14. The semiconductor package of claim 13 comprises:

a top RDL layer on a top surface of the encapsulated die; and

a bottom RDL layer on a bottom surface of the encapsulated die, wherein the RDL layers and the at least one through-via facilitates stacking of packages.

15. The semiconductor package of claim 13 wherein the die includes first and second die surfaces, wherein the first die surface is an active surface and the first die surface is coplanar with a first surface of the mold compound.

16. The semiconductor package of claim 15 wherein the second die surface is an inactive surface and the second die surface is coplanar with a second surface of the mold compound and the inactive surface of the die is exposed.

17. The semiconductor package of claim 9 wherein the structural member and the mold compound are separate components and comprise the same material.

18. The semiconductor package of claim 17 wherein the at least one through-via extends through the mold compound and the first and second major surfaces of the structural member.

19. The semiconductor package of claim 17 wherein the die includes first and second die surfaces, wherein the first die surface is an active surface and the first die surface is coplanar with a first surface of the mold compound.

20. The semiconductor package of claim 19 comprises:

a top RDL layer on a top surface of the encapsulated die; and

a bottom RDL layer on a bottom surface of the encapsulated die, wherein the RDL layers and the at least one through-via facilitates stacking of packages.