Claims:

1. A substrate support configured to support a semiconductor substrate in a semiconductor processing apparatus, the substrate support comprising:

an electrically insulating layer;

a plurality of planar thermal zones each comprising one or more thermal elements made of an insulator-conductor composite, the planar thermal zones laterally distributed across the electrically insulating layer;

power supply lines comprising at least a first electrically conductive power supply line electrically connected to at least two of the planar thermal zones and a second electrically conductive power supply line electrically connected to at least two of the planar thermal zones;

power return lines comprising at least a first electrically conductive power return line electrically connected to at least two of the planar thermal zones and a second electrically conductive power return line electrically connected to at least two of the planar thermal zones;

wherein each planar thermal zone is connected to a different pair of power supply and return lines, wherein the power supply lines and the power return lines are on a different plane than the plurality of planar thermal zones, and wherein respective widths of the power supply lines and the power return lines are as large as a width of the plurality of planer thermal zones.

2. The substrate support of claim 1, wherein the insulator-conductor composite comprises one or more insulator materials selected from the group consisting of Al_2O_3, SiO_2, Si_3N_4 and AlN, and one or more conductor materials selected from the group consisting of Al, Cu, Mo, W, Au, Ag, Pt, Pd, C, $MoSi_2$, WC and SiC.

3. The substrate support of claim 2, wherein the insulator-conductor composite comprises up to 30 wt % of Al_2O_3 and balance of W.

4. The substrate support of claim 1, wherein the planar thermal zones are sized such that:

(a) each planar thermal zone has a cross-sectional area of 0.1 to 1 cm^2,

(b) each planar thermal zone has a cross-sectional area of 1 to 3 cm^2,

(c) each planar thermal zone has a cross-sectional area of 3 to 15 cm^2, or

(d) each planar thermal zone has a cross-sectional area of 15 to 100 cm^2.

5. The substrate support of claim 1 includes 100 to 1000 thermal zones wherein each thermal element has a serpentine shape.

6. The substrate support of claim 1, wherein the electrically insulating layer comprises a polymer material, a ceramic material, a fiberglass composite, or a combination thereof.

7. The substrate support of claim 1, wherein the total number of the power supply lines and the power return lines is equal to or less than the total number of the planar thermal zones.

8. The substrate support of claim 1, wherein a total area of the planar thermal zones is from 50% to 99% of an upper surface of the substrate support.

9. The substrate support of claim 1, wherein the planar thermal zones are arranged in a rectangular grid, hexagonal grid or concentric rings; and the thermal zones are separated from each other by gaps at least 1 millimeter in width and at most 10 millimeters in width.

10. A substrate support comprising an electrostatic chuck (ESC) configured to provide support to a semiconductor substrate in a semiconductor processing chamber, the ESC comprising:

an electrically insulating layer;

a plurality of planar thermal zones each comprising one or more thermal elements made of an insulator-conductor composite, the planar thermal zones laterally distributed across the electrically insulating layer;

power supply lines comprising at least a first electrically conductive power supply line electrically connected to at least two of the planar thermal zones and a second electrically conductive power supply line electrically connected to at least two of the planar thermal zones;

power return lines comprising at least a first electrically conductive power return line electrically connected to at least two of the planar thermal zones and a second electrically conductive power return line electrically connected to at least two of the planar thermal zones;

wherein each planar thermal zone is connected to a different pair of power supply and return lines; and

a cooling plate configured to provide a heat sink beneath the ESC, wherein the power supply lines and the power return lines are on a different plane than the plurality of planar thermal zones, and wherein respective widths of the power supply lines and the power return lines are as large as a width of the plurality of planer thermal zones.

11. The substrate support of claim 10, further comprising at least one primary thermal layer disposed above or below the planar thermal zones, wherein the primary thermal layer is electrically insulated from the planar thermal zones, the power supply lines, and the power return lines of the ESC.

12. The substrate support of claim 11, wherein the primary thermal layer includes two or more primary thermal elements powered with at least 100 W.

13. A method of making a substrate support comprising an electrically insulating layer, a plurality of planar thermal zones each comprising one or more thermal elements made of an insulator-conductor composite, the planar thermal zones laterally distributed across the electrically insulating layer, power supply lines comprising at least a first electrically conductive power supply line electrically connected to at least two of the planar thermal zones and a second electrically conductive power supply line electrically connected to at least two of the planar thermal zones, power return lines comprising at least a first electrically conductive power return line electrically connected to at least

two of the planar thermal zones and a second electrically conductive power return line electrically connected to at least two of the planar thermal zones, wherein each planar thermal zone is connected to a different pair of power supply and return lines, wherein the power supply lines and the power return lines are on a different plane than the plurality of planar thermal zones, and wherein respective widths of the power supply lines and the power return lines are as large as a width of the plurality of planer thermal zones, the method comprising:

mixing powders of an insulator and a conductor with a liquid into a slurry, screen printing the slurry on the electrically insulating layer and sintering the slurry.

14. The method of claim 13, wherein the liquid is selected from the group consisting of methanol, ethanol, acetone, isopropyl alcohol, water, mineral oil and a mixture thereof.

15. The method of claim 13, wherein the powders have particle sizes from 0.2 to 20 microns.

16. A method for manufacturing a substrate support comprising an electrically insulating layer, a plurality of planar thermal zones each comprising one or more thermal elements made of an insulator-conductor composite, the planar thermal zones laterally distributed across the electrically insulating layer, power supply lines comprising at least a first electrically conductive power supply line electrically connected to at least two of the thermal zones and a second electrically conductive power supply line electrically connected to at least two of the thermal zones, power return lines comprising at least a first electrically conductive power return line electrically connected to at least two of the thermal zones and a second electrically conductive power return line electrically connected to at least two of the thermal zones, wherein each thermal zone is connected to a different pair of power supply and return lines, wherein the power supply lines and the power return lines are on a different plane than the plurality of thermal zones, and wherein respective widths of the power supply lines and the power return lines are as large as a width of the plurality of planer thermal zones, the method comprising:

pressing a mixture of ceramic powder, binder and liquid into sheets;

drying the sheets;

forming vias in the sheets by punching holes therein;

forming the power supply lines and power return lines on the sheets;

forming the thermal elements by screen printing or spraying a slurry of insulator and conductor powders;

aligning the sheets;

bonding the sheets together by sintering to form the electrically insulating layer;

filling the vias with a slurry of conducting powder.

17. The method of claim 16, wherein the power supply lines and power return lines are formed by screen printing a slurry of conducting powder, pressing a precut metal foil, or spraying a slurry of conducting powder.

18. A method for plasma processing semiconductor substrates in a plasma processing chamber containing a substrate support with an electrostatic chuck comprising an electrically insulating layer, a plurality of planar thermal zones each comprising one or more thermal elements made of an insulator-conductor composite, the planar thermal zones laterally distributed across the electrically insulating layer, power supply lines comprising at least a first electrically conductive power supply line electrically connected to at least two of the planar thermal zones and a second electrically conductive power supply line electrically connected to at least two of the planar thermal zones, power return lines comprising at least a first electrically conductive power return line electrically connected to at least two of the planar thermal zones and a second electrically conductive power return line electrically connected to at least two of the planar thermal zones, wherein each planar thermal zone is connected to a different pair of power supply and return lines, wherein the power supply lines and the power return lines are on a different plane than the plurality of planar thermal zones, wherein respective widths of the power supply lines and the power return lines are as large as a width of the plurality of planer thermal zones, the method comprising:

(a) loading a semiconductor substrate into the processing chamber and positioning the semiconductor substrate on the substrate support;

(b) determining a temperature profile that compensates for processing conditions affecting critical dimension (CD) uniformity;

(c) heating the semiconductor substrate to conform to the temperature profile using the substrate support;

(d) igniting plasma and processing the semiconductor substrate while controlling the temperature profile by independently controlled temperature of the planar thermal zones;

(e) unloading the semiconductor substrate from the processing chamber and repeating steps (a)-(e) with a different semiconductor substrate.