

WHAT IS CLAIMED IS:

1. A memory device, comprising:
 - a first layer stack having first alternating conductor and insulator layers;
 - a top dielectric layer disposed on the first layer stack;
 - a second layer stack, disposed over the top dielectric layer and having second alternating conductor and insulator layers;
 - one or more first vertical structures extending through the first layer stack;
 - one or more second vertical structures extending through the second layer stack and at least a portion of the top dielectric layer; and
 - a conductive material sandwiched between the one or more first vertical structures and the one or more second vertical structures, wherein
 - a width of the conductive material is greater than a width of the one or more second vertical structures contacting the conductive material.
2. The memory device of claim 1, wherein the one or more first vertical structures comprise one or more first NAND strings and the one or more second vertical structures comprise one or more second NAND strings.
3. The memory device of claim 2, wherein each of the one or more first NAND strings and each of the one or more second NAND strings includes a plurality of memory layers surrounding a core insulating material.
4. The memory device of claim 3, wherein the plurality of memory layers includes a stack consisting of a blocking layer, a storage layer, a tunneling layer, and a channel layer.
5. The memory device of claim 4, wherein dopants originating from the conductive material are present in portions of the channel layer adjacent to the conductive material.
6. The memory device of claim 4, wherein the conductive material is disposed over a recess on a top portion of the one or more first NAND strings and is in contact with the blocking

layer, the storage layer, the tunneling layer, and the channel layer of the one or more first NAND strings.

7. The memory device of claim 4, wherein the one or more second NAND strings further comprise a nested recess over the conductive material, the nested recess extending through the blocking layer, the storage layer and tunneling layer.
8. The memory device of claim 7, wherein the channel layer of the one or more second NAND strings is disposed over the nested recess, forming an ohmic contact with the conductive material.
9. The memory device of claim 4, wherein the one or more second vertical structures further comprise a top conductive material in a top portion, the top conductive material electrically connected to the channel layer of the one or more second vertical structures.
10. The memory device of claim 9, wherein the top conductive material comprises polysilicon.
11. The memory device of claim 9, wherein dopants originating from the top conductive material are present in portions of the channel layer adjacent to the top conductive material.
12. The memory device of claim 1, wherein a portion of the conductive material surrounds a lower end of the one or more second vertical structures.
13. The memory device of claim 1, wherein a width of the conductive material is greater than a width of the one or more first vertical structures contacting the conductive material.
14. The memory device of claim 1, wherein the conductive material projects outward from the one or more first vertical structures and the one or more second vertical structures.

15. The memory device of claim 1, wherein the one or more second vertical structures extend through a portion of the conductive material.
16. The memory device of claim 1, wherein the top dielectric layer surrounds the conductive material.
17. The memory device of claim 1, wherein the conductive material is configured to provide electrical connection between the one or more first vertical structures and the one or more second vertical structures.
18. The memory device of claim 1, wherein the conductive material comprises polysilicon.
19. The memory device of claim 1, further comprising:
 - a first staircase structure formed in the first layer stack; and
 - a second staircase structure formed in the second layer stack.
20. The memory device of claim 19, wherein at least one of the one or more first vertical structures extend through the first staircase structure; and at least one of the one or more second vertical structures extend through the second staircase structure.