CLAIMS

1. A method of manufacturing a micro-light emitting diode (uLED) device comprising:

depositing a plurality of semiconductor layers including an n-type layer, an active layer, and a p-type layer on a substrate;

depositing a p-contact layer on the plurality of semiconductor layers;

depositing a hard mask layer on the p-contact layer;

etching a portion of the semiconductor layers, the p-contact layer, and the hard mask layer to form trenches and plurality of mesas, each of the mesas having a height spanning from a top surface of the p-contact layer to a bottom surface of the n-type layer and a width spanning a first sidewall of the n-type layer to a second sidewall of the n-type layer;

depositing a dielectric material over the substrate into the trenches and on an uppermost surface of the substrate;

first etching to expose the p-contact layer and a first portion of a surface of the substrate;

second etching to expose the n-type layer and a second portion of the surface of the substrate;

depositing a first metal onto areas exposed by the first etching and the second etching; and

etching to form a cathode and an anode which are isolated from each other;

the foregoing steps forming a processed structure.

2. The method of claim 1, wherein the width of the mesa is less than 100 micrometers.

3. The method of claim 1, wherein the height of the mesa is less than or equal to the width of the mesa.

4. The method of claim 1, wherein the first etching and/or the second etching independently comprise anisotropic etching.

5. The method of claim 1 comprising conducting a masking prior to the etching to expose the p-contact layer.

6. The method of claim 1, wherein two planar orientations of the p-contact layer are exposed during the etching to expose the p-contact layer.

7. The method of claim 1, wherein two planar orientations of the n-type layer are exposed during the etching to expose the n-type layer.

8. The method of claim 1 comprising conducting a masking prior to the etching to expose the n-type layer.

9. The method of claim 1 comprising forming a passivation layer on the processed structure.

10. The method of claim 1 comprising adhering bonding surfaces of the cathode and the anode to a support; removing the substrate; and singulating the mesas to form individual uLED devices.

11. The method of claim 1, wherein the n-type layer comprises N-GaN and the p-type layer comprises P-GaN.

12. The method of claim 1, wherein a first region of dielectric material insulates the p-contact layer, the active layer, and a first sidewall of the p-type layer from the cathode, and a second region of dielectric material insulates the active layer, a second sidewall of the p-type layer, and the second sidewall of the n-type layer from the anode; and the dielectric material of the first region and of the second region independently each comprise a material selected from the group consisting of SiO_2, AlO_x, and SiN, each independently has a thickness in a range of from 200 nm to 1 μm.

13. The method of claim 1, wherein the p-contact layer contacting the p-type layer substantially spans a width of the p-type layer.

14. The method of claim 1, wherein the p-type layer substantially spans a width of the active layer.

15. A method of making a display device comprising:

attaching plurality of micro light emitting diodes (uLEDs) to a backplane by a pick-and-place method; and

enclosing the plurality of uLEDs in a housing with a display face;

each of the uLEDS comprising:

a mesa comprising:

a plurality of semiconductor layers including an n-type layer, an active layer, and a p-type layer;

a p-contact layer contacting the p-type layer;

the mesa comprising a height spanning from a top surface of the p-contact layer to a bottom surface of the n-type layer and a width spanning a first sidewall of the n-type layer to a second sidewall of the n-type layer; the top surface of the p-contact layer having a different planar orientation compared to the first and second sidewalls of the n-type layer;

a cathode contacting the first sidewall of the n-type layer;

a first region of dielectric material that insulates the p-contact layer, the active layer, and a first sidewall of the p-type layer from the cathode;

an anode contacting the top surface of the p-contact layer; and

a second region of dielectric material that insulates the active layer, a second sidewall of the p-type layer, and the second sidewall of the n-type layer from the anode.

16. The method of claim 15, wherein the width of the mesa is less than 100 micrometers.

17. The method of claim 15, wherein the height of the mesa is less than or equal to the width of the mesa.

18. The method of claim 15, wherein the p-contact layer contacting the p-type layer substantially spans a width of the p-type layer.

19. The method of claim 15, wherein the p-type layer substantially spans a width of the active layer.