Description

This invention relates to semiconductor integrated circuits, and more particularly to a scheme for arranging interconnecting metallization lines in such circuits.

Semiconductor integrated circuits typically are formed by MOS (metal oxide semiconductor) or by bipolar transistors that are integrated at a top planar major surface of a silicon chip. Electrical interconnections between various transistors, as well as between certain transistors and access pins typically located along the periphery of the chip, have typically taken the form of two (or more) "levels" of interconnections, i.e., electrically conducting lines in the form of metallization stripes running along two (or more) essentially planar surfaces that are oriented mutually parallel to both each other and the top planar surface of the chip. These levels are insulated from one another and from the top surface of the chip by insulating layers. Interconnection vias (windows) in the insulating layers are provided wherever they are needed in accordance with the desired circuit interconnections between levels.

In a variety of such integrated circuit-such as random access memories (RAM) and logic circuit-the electrical circuit requires interconnections by means of a number of electrically conducting lines which conveniently are topologically arranged in the form of an array of mutually parallel metallization stripes. For example, in a DRAM (dynamic RAM) there is an array of parallel word line-each word line enabling access to a separate group of bits via an array of bit lines perpendicular to the word lines. Typically, a DRAM contains hundreds (or more) of these parallel word lines and hundreds (or more) of these bit lines. Unavoidable parasitic capacitance across each pair of neighboring word lines gives rise to the problem of noise caused by the resulting electrical cross-coupling or "cross-talk" between such word lines. Because of this cross-coupling, desired electrical access to any given word line-for the purpose of enabling the writing of new information (corresponding to a new word) into the given word line or for reading the existing information stored in the selected line of the memory--results in undesired spurious access to, and consequent spurious writing or reading of information into or out of, the non-accessed neighboring word(s). That is, access to any given word line may spuriously influence the stored charge in the memory cells of the neighboring word line(s) that is (are) supposedly not being accessed. The term "pattern sensitivity" has been applied to this undesirable phenomenon. A similar noise problem can be encountered in a parallel array of bit lines. Similarly, in other integrated circuits such as logic circuits, parasitic cross-coupling between neighboring lines--such as lines of a bus, as used for routing of interconnections--can give rise to spurious electrical cross-talk between neighboring lines. This cross-talk reduces the sensitivity of the original detection and can result in errors. Accordingly, it would be desirable to have an arrangement of lines that reduces parasitic cross-coupling between them.

IEEE Journal of Solid State Circuits, Vol. SC-16, No. 4, August 1981, pages 293 to 301 discloses an array as defined in the first part (or preamble) of claim 1.

According to the present invention, there is provided a circuit as defined in claim 1.

Parasitic cross-coupling between neighboring interconnecting lines in a semiconductor integrated-circuit--such as between neighboring word lines in a DRAM--is reduced by the use of "marching" lines. By "marching" it is meant that the lines are topologically arranged in a given progressive marching sequence, whereby a line has, at least on one side thereof, as its next neighboring line a different one of the other lines. In an array of lines in the XY plane arranged for transmitting signals along the X direction, each line runs to form a first segment along the X direction at constant Y coordinate for only a relatively short first distance (as compared with the total length of the line), then marches to a new Y coordinate, and then runs to form a second segment along the X direction at the new Y coordinate for only a relatively short second distance, then marches to another new Y coordinate, and so forth. In this way, the identity of the next neighboring lines on both sides of any given line keeps changing from segment to segment. Thereby the parasitic capacitance between any pair of lines is significantly reduced, because the parasitic capacitance between a given line and other next neighboring lines is thereby distributed, and hence dissipated, among many other such lines, instead of cumulating among just two other (fixed) neighboring lines as in prior art. The lines themselves can serve as the word lines (or the bit lines) in & memory circuit such as a DRAM, as bus lines of a data bus in a microprocessor or other logic circuit, or as any other interconnecting lines in parallel array of conducting lines in an integrated circuit.

Brief Description of the Drawing

FIG. 1 is a stick diagram showing the physical layout of an illustrative portion of an array of marching interconnecting lines in accordance with an embodiment of the invention; and

FIG. 2 is a stick diagram showing the physical layout of an illustrative portion of an array of

marching interconnecting lines in accordance with another embodiment.

Only for the sake of clarity the figures are not drawn to any scale.

FIG. 1 shows an array 100 of electrically conducting lines 1,2,3,...12 in an integrated circuit (not shown), in accordance with an embodiment of the invention. The (odd-numbered) line 1, for example, starts at the upper-lefthand corner, runs for a distance L_1, in the X direction to form a first segment, then marches in the -Y direction for a distance W_1, while running in the X direction for a distance d_1, and so forth, until it reaches the extreme righthand edge of FIG. 1. On the other hand, the (even-numbered) line 2 starts at a position located at the left-hand edge at a distance W_1 as measured in the -Y direction from the extreme left-hand-edge of the line 1, runs for a distance L_1 in the X direction, marches in the +Y direction for the distance W_1, while running in the X direction for the distance d_1, then runs along the X direction for a distance $(L_2 + d_2 + L_3)$, in the -Y direction for the distance W_1 while running along the X direction for a distance d_3, and continues in this (X, -Y) manner until it reaches the extreme right-hand-edge of the layout. Cross-coupling parasitic capacitances C_{12}, C_{21}, etc., between neighboring segments of adjacent lines are indicated by dotted lines. For clarity, not all parasitic capacitors are shown in FIG. 1. It should be understood, of course, that the layout of the array 100 in general can and generally will extend farther in both the X and Y directions than actually shown, to form a regular pattern. Thus FIG. 1 shows only an illustrative portion of an array of marching lines.

In general, as seen in FIG. 1, each even-numbered line begins its march in the +Y direction as it runs along the X direction and continues its march in the +Y direction unless and until it reaches the top extremity (Y = maximum)--in which case it marches thereafter in the -Y direction as it runs still farther along the X direction. Similarly, an odd-numbered line begins its march in the -Y direction, and when the line reaches the bottom extremity (-Y = maximum) it marches thereafter in the +Y direction as it runs still farther along the +X direction after pausing in the Y direction for a distance $(L_i + d_i + L_{i+1})$ along the X direction, where i is an integer corresponding to the position (along the X direction) of the bottom extremity. It should be clear from the illustration that one half of the lines are marching in the +Y direction while the other half marches in the -Y direction at any given location X of the array, except that when a line reaches the upper (+Y) or lower (-Y) extremity of the array, it begins marching in the opposite direction, as previously described.

For the sake of orderliness and regularity (but not essential to the goal of decreasing parasitic coupling) all L's are made equal, as are all W's and all d's: $L_1 = L_2 = L_3 = ...$; $W_1 = W_2 = W_3 = ...$; and $d_1 = d_2 = d_3 = ...$ In practice, each of the L's would be a sufficiently small fraction of the overall line length so that there are many crossovers per line and hence sufficient dispersion of the parasitic capacitance, the W's would be governed by the particular design or layout, and the d's would be determined by the particular means of crossing lines. Note that, for a typical example, the cross-coupling parasitic capacitance $(C_{12} + C_{21})$ between lines 1 and 2 is relatively small as compared to what it would be in prior art where these lines would be situated close together and geometrically parallel throughout their total extents in the X direction, because of the relatively small running distance $(L_1 + d_1 + L_2)$ of close approach in accordance with this invention as compared with the prior art's running distance of close approach equal to the total extent of the lines 1 and 2--it being understood that all the lines 1,2,...12 can, and typically do, extend much farther in the ±X direction than is actually shown in FIG. 1.

The maximum number of crossovers $(d_1, d_2, d_3...)$ should advantageously equal one less than the total number of lines. The implementation with the number of crossovers equal to one less than the number of lines provide the maximum dispersion and hence reduction of coupling capacitance, with each line having an equal amount of coupling capacitance to every other line.

It should be further understood that crossings of adjacent lines are realized in an integrated circuit by means of standard cross-over techniques utilizing two (or more) levels of interconnect metallization in which cross-overs are formed typically where one of the lines locally crosses over (or under) a second line by means of a second level of interconnection, while the second line maintains itself on the same metallization level and marches (up or down) to its new Y positions. Two windows and one crossover (or crossunder) segment are ordinarily used for each d_i interval.

The embodiment shown in FIG. 1 is a particularly orderly scheme for reducing (and minimizing) nearest neighbor crosstalk to other lines in the array. FIG. 2 shows another embodiment 200, for achieving a similar beneficial result in accordance with the invention, having triple crossovers at each d_i interval.

Claims

1. An array of interconnection lines in a semiconductor integrated circuit comprising a multiplicity of metallization lines located on a surface of a semiconductor body within a metallization

marching interconnecting lines in accordance with another embodiment.

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Claims

1. An array of interconnection lines in a semiconductor integrated circuit comprising a multiplicity of metallization lines located on a surface of a semiconductor body within a metallization

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area bounded by a pair of parallel edges extending in a direction x, all the lines being mutually parallel and parallel to said edges everywhere except in a plurality of separate crossing regions in each of which every line crosses at least one other line by marching in a direction Y transverse to the X direction, this marching being reversed once a line has reached one of the parallel edges, whereby each of the lines is divided into a plurality of mutually parallel segments each of which runs between successive crossing regions in the X direction, CHARACTERISED IN THAT the marching direction of even numbered lines in the crossing regions is opposite to the marching direction of odd numbered lines of the array.

Revendications

1. Un réseau de lignes d'interconnexion dans un circuit intégré à semiconducteurs, comprenant un ensemble de lignes de métallisation situées sur une surface d'un bloc de semiconducteur, dans une zone de métallisation qui est limitée par une paire de bords parallèles s'étendant dans une direction X, toutes les lignes étant mutuellement parallèles et parallèles aux bords précités, partout sauf dans un ensemble de régions de croisement séparées, dans chacune desquelles chaque ligne croise au moins une autre ligne en progressant dans une direction Y qui est transversale à la direction X, cette progression étant inversée une fois qu'une ligne a atteint l'un des bords parallèles, grâce à quoi chacune des lignes est divisée en un ensemble de segments mutuellement parallèles, chacun d'eux s'étendant entre des régions de croisement successives dans la direction X, CARACTERISE EN CE QUE la direction de progression de lignes paires dans les régions de croisement est opposée à la direction de progression de lignes impaires du réseau.

Patentansprüche

1. Anordnung von verbindungsleitungen in einer integrierten Halbleiterschaltung mit einer Vielzahl von sich in einer Richtung X erstreckender Metallisierungsleitungen auf einer Oberfläche eines Halbleiterkörpers in einem durch ein Paar paralleler Kanten begrenzten Metallisierungsbereich, wobei alle Leitungen gegenseitig parallel und parallel zu den Kanten überall mit Ausnahme von getrennten Kreuzungsbereichen verlaufen, in denen jeweils jede Leitung wenigstens eine andere Leitung durch Querversatz in einer Richtung Y quer zur X-Richtung kreuzt und dieser Querversatz umgekehrt wird, wenn eine Leitung eine der parallelen Kanten erreicht, wodurch jede Leitung in eine vielzahl gegenseitig paralleler Abschnitte unterteilt ist, die je zwischen aufeinander folgenden Kreuzungsbereichen in der X-Richtung verlaufen, dadurch gekennzeichnet,
daß die Querversatzrichtung gerade nummerierter Leitungen in den Kreuzungsbereichen entgegengesetzt zu der Querversatzrichtung ungerade nummerierter Leitungen der Anordnung ist.

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