ABSTRACT

A method of forming a gate electrode, comprising the following steps. A semiconductor substrate having an overlying patterned layer exposing a portion of the substrate within active area and patterned layer opening. The patterned layer having exposed sidewalls. Internal spacers are formed over a portion of the exposed substrate portion within the patterned layer opening on the patterned layer exposed sidewalls. The internal spacers being comprised of a WF1 material having a first work function. A planarized gate electrode body is formed within the remaining portion of the patterned layer opening and adjacent to the internal spacers. The gate electrode body being comprised of a WF2 material having a second work function. The internal spacers and the gate electrode body forming the gate electrode.

Fig 4