

PATENT SPECIFICATION

(11) 1 570 162

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(21) Application No. 17997/78. (22) Filed 5 May 1978

(31) Convention Application No. 52/060108

(32) Filed 23 May 1977 in

(33) Japan (JP)

(44) Complete Specification published 25 June 1980

(51) INT CL³ G04C 21/28

(52) Index at acceptance

G3T 608 609 611 S1

G4D 442 AA

G5J 1T2 2F1



(54) AN ALARM ELECTRONIC TIMEPIECE

(71) We, KABUSHIKI KAISHA DAINI SEIKOSHA, a Japanese body corporate of 6-31-1, Kameido, Koto-ku, Tokyo, Japan, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed to be particularly described in and by the following statement:—

This invention relates to alarm electronic timepieces.

According to the present invention there is provided an alarm electronic timepiece comprising: time keeping means for producing timing signals; a display device connected to receive the timing signals and to display an actual time of day; alarm setting means for memorising a predetermined alarm time and for producing an alarm set signal when the alarm time and the actual time of day coincide; audible warning means which is rendered operative by the alarm set signal; and alarm signal generating means including first means for producing a plurality of audio frequency signals having different duty cycles and second means for combining the audio frequency signals to produce an alarm signal whose amplitude varies with time and which causes the audible warning means, when operative, to produce an audible warning.

The time keeping means may include an oscillator circuit for generating a standard time signal.

The timepiece may be arranged such that, when the standard time signal has a frequency f_0 and the audio frequency signals each have the same frequency f_A , the minimum duty cycle of the audio frequency signals is $f_A/2f_0$.

Preferably the time keeping means includes a frequency divider circuit having a plurality of divider stages for frequency dividing the standard time signal, the generating means being connected to receive a plurality of signals of different frequencies from the divider circuit and to

produce the audio frequency signals therefrom.

In a preferred embodiment the generating means is such that the alarm signal decreases in amplitude with time.

The second means may be arranged to produce a cyclically amplitude varying alarm signal. Thus the second means may include a ring counter whose rate of counting is controlled, in operation, by a signal from the time keeping means.

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:—

Figure 1 illustrates a conventional alarm generating circuit for an alarm electronic timepiece;

Figures 2 and 3 illustrate the operation of the alarm generating circuit of Figure 1;

Figure 4 is a block diagram of one embodiment of an alarm electronic timepiece according to the present invention;

Figure 5 is a circuit diagram of a divider circuit of the alarm electronic timepiece of Figure 4;

Figure 6 is a circuit diagram of an alarm signal generating circuit and a driving circuit of an alarm electronic timepiece of Figure 4;

Figure 7 is a timing chart illustrating the operation of the divider circuit shown in Figure 5;

Figures 8 to 11 are timing charts illustrating the operation of the alarm signal generating circuit shown in Figure 6;

Figure 12 is a model diagram illustrating the alarm signal produced by the alarm signal generating circuit of Figure 6;

Figure 13 illustrates a modification of the alarm signal generating circuit of Figure 6;

Figure 14 is a model diagram of the alarm signal produced by the alarm signal generating circuit modified in accordance with Figure 13;

Figure 15 is a characteristic diagram showing the relationship between the duty cycle of the alarm signal shown in Figure 12

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and sound pressure for an electro-magnetic speaker of the alarm electronic timepiece with Figure 4;

5 Figure 16 illustrates a variation of sound pressure with time of the audible sound generated by the alarm signal generating circuit of Figure 6; and

10 Figure 17 illustrates the variation of sound pressure with time of the audible sound generated by the alarm signal generating circuit of Figure 13.

Generally, electronic timepieces display an actual time of day by frequency dividing a standard or reference time signal produced by, for example, a quartz crystal oscillator. In an alarm electronic timepiece, it is convenient to use, as an alarm signal, a signal produced in a part of a time-keeping circuit, the alarm signal driving a sounding body, e.g. a buzzer or speaker.

20 Figure 1 illustrates a conventional alarm generating circuit in which an audible signal (Figure 2(A)) having a frequency of 4096Hz and an interrupting signal (Figure 2(B)) having a frequency of 8Hz are produced from frequency divider stages of a time keeping circuit and fed to inputs of an AND circuit 101. An alarm signal (Figure 2(C)) from the output of the AND circuit 101 and an alarm set signal are fed to inputs of an AND circuit 102. The output signal from the AND circuit 102 is connected to the base of a transistor 72. A speaker 14 is connected to a collector of the transistor 72. In operation, the alarm signal from the AND circuit 101 is composed of the audible signal modulated by the interrupting signal and this alarm signal is fed to the base of the transistor 72 through the AND circuit 102 when the alarm set signal is at a high level with the result that the speaker 14 is energised. The alarm set signal is a signal produced when an alarm is to be given, for instance, when a predetermined alarm time and an actual time of day coincide. The wave shape of the sound wave produced from the speaker 14 is as shown in Figure 3. The advantage of an intermittent alarm sound is that it breaks the monotony of a continuous alarm sound, but it may give listeners an unpleasant feeling since it is substantially in the form of a square wave.

Referring now to Figure 4, there is shown, in block diagram form, one embodiment of an alarm electronic timepiece according to the present invention. An output signal from an oscillator circuit 1 is fed to a frequency divider circuit 2 and the output signal therefrom is successively fed to a seconds counter 3, a minutes counter 4, an hours counter 5 and a days counter 6. The contents of the seconds counter 3, the minutes counter 4, the hours counter 5 and the days counter 6 are respectively fed to a decoder/driver circuit 7 which drives a time

display device 8. The content of the minutes counter 4 and the hours counter 5 are also fed to a coincidence circuit 9. The contents of an alarm minutes memory circuit 10 and an alarm hours memory circuit 11 are also fed to the coincidence circuit 9. An alarm set signal from the coincidence circuit 9 is fed to an alarm signal generating circuit 12. Output signals from intermediate stages of the divider circuit 2 are also fed to the generating circuit 12 which produces an alarm signal which is fed to a driving circuit 13 which drives a speaker 14.

The operation of the alarm electronic timepiece of Figure 4 is as follows. The oscillator circuit 1 generates a standard or reference time signal having a frequency of, for example, 32,768Hz with a rectangular waveform. The divider circuit 2 is composed of a plurality of flip-flop stages and frequency divides the reference time signal to produce an output signal having a frequency of 1Hz. The output signal from the divider circuit 2 is fed to the seconds counter 3 consisting of a 60-step counter to count seconds and a figure-up or carry signal from the seconds counter 3 is fed to the minutes counter 4 which also consists of a 60-step counter for counting minutes. A carry signal from the minutes counter 4 is fed to the hours counter 5 which consists of a 24-step counter for counting hours. A carry signal from the hours counter 5 is fed to the days counter 6 which counts the days. Bit signals from the seconds counter 3, the minutes counter 4, the hours counter 5 and the days counter 6 are fed to the decoder/driver circuit 7 which decodes the bit signals and drives the display device 8. The display device 8 is composed of display elements such as liquid crystals, light emitting diodes etc., and displays the actual time of day in seconds, minutes, hours and days.

The coincidence circuit 9 produces an alarm set signal of high level when the contents of the minutes counter 4 and the alarm minutes memory circuit 10 coincide and when the contents of the hours counter 5 and the alarm hours memory circuit 11 coincide respectively. That is to say, the alarm set signal is produced when the alarm time set in the memory circuits 10, 11 and the minutes and hours of the actual time of day coincide.

The generating circuit 12 is a main part of the present invention and will be described in greater detail hereinafter. The generating circuit 12 produces a plurality of signals having different duty cycles from signals obtained from intermediate stages of the divider circuit 2 and combines them to produce an alarm signal for driving the speaker 14 when the alarm set signal is produced. The alarm signal from the

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generating circuit 12 is fed to the driving circuit 13 to drive the speaker 14. The basic construction and operation of an alarm electronic timepiece according to the present invention have been illustrated so far. Time correcting circuitry, alarm time setting circuitry and other conventional features of electronic timepieces are not shown or described since these are not directly relevant to the present invention.

Figure 5 shows the divider circuit 2 in greater detail. An output signal Q_0 from the oscillator circuit 1 is fed to an inverter 20, wherefrom an output signal $\bar{Q}_0$ is fed to a flip-flop stage 21. An output signal $\bar{Q}_1$ from the flip-flop stage 21 is fed to a flip-flop stage 22. Flip-flop stages 23 to 35 are connected as shown in Figure 5. Each flip-flop stage divides the frequency of its input signal by one half. Accordingly, as shown in Figure 7, the signal Q_0 , which has a frequency of 32,768Hz is frequency divided so that a signal Q_1 has a frequency of 16,384Hz, signal Q_2 has a frequency of 8,192Hz, a signal Q_3 has a frequency of 4,096Hz, etc. Signals Q_1 , Q_2 , Q_3 are respectively the output signals of the flip-flop stages 21, 22, 23. An output signal Q_{15} from the flip-flop stage 35 has a frequency of 1Hz. Thus the frequency divider circuit frequency divides the input signal by $1/2^n$, where n is the number of flip-flop stages in the divider circuit.

Referring now to Figure 6, the alarm signal generating circuit 12 and the driving circuit 13 are illustrated in greater detail. The signals Q_0 , $\bar{Q}_0$, Q_1 , $\bar{Q}_1$, Q_2 , $\bar{Q}_2$, Q_3 , $\bar{Q}_3$ from the divider circuit 2 are fed to the generating circuit 12. The generating circuit has 4-input AND circuits 41 to 48. Signals $\bar{Q}_0$, Q_1 , Q_2 , Q_3 are fed to the AND circuit 41, signals Q_0 , Q_1 , Q_2 , Q_3 are fed to the AND circuit 42, signals Q_0 , $\bar{Q}_1$, Q_2 , Q_3 are fed to the AND circuit 43, signals Q_0 , Q_1 , $\bar{Q}_2$, Q_3 are fed to the AND circuit 44, signals $\bar{Q}_0$, Q_1 , $\bar{Q}_2$, Q_3 are fed to the AND circuit 45, signals Q_0 , Q_1 , Q_2 , $\bar{Q}_3$ are fed to the AND circuit 46, signals Q_0 , $\bar{Q}_1$, $\bar{Q}_2$, Q_3 are fed to the AND circuit 47, and signals Q_0 , Q_1 , Q_2 , $\bar{Q}_3$ are fed to the AND circuit 48. Output signals D_1 , D_2 , D_3 , D_4 , D_5 , D_6 , D_7 , D_8 produced from the AND circuits 41 to 48 are fed to a reset terminal R of a D-type flip-flop 70 through respective transmission gates 51 to 58. A 16-step ring counter 80 receives, at a clock terminal CL, an output signal $\bar{Q}_{11}$ (frequency 16Hz) from the flip-flop stage 31 of the divider circuit 2. Output signals Q_A , Q_B , Q_C , Q_D , Q_E from the ring counter 80 are respectively connected to junction points T_8 , T_7 , T_6 , T_5 , T_4 , output signals Q_F , Q_G are fed to an OR circuit 81, output signals Q_H , Q_I , Q_J are fed to an OR circuit 82 and output signals Q_K , Q_L , Q_M , Q_N , Q_O , Q_P are fed to an OR circuit 83.

The output signals from the OR circuits 81, 82, 83 are respectively connected to junction points T_3 , T_2 , T_1 . The junction point T_1 is connected to an N-channel gate of the transmission gate 51 and also to a P-channel gate of the transmission gate 51 through an inverter 61. Likewise, the junction points T_2 , T_3 , T_4 , T_5 , T_6 , T_7 , T_8 are connected to respective N-channel gates of the transmission gates 52 to 58 and also to respective P-channel gates thereof through inverters 62 to 68. The signal Q_3 is fed to a data terminal of the flip-flop 70 and the signal Q_2 is fed to a clock terminal CL thereof. An alarm signal from the flip-flop 70 is fed to one input of an AND circuit 71. The alarm set signal from the coincidence circuit 9 is fed to the other input of the AND circuit 71.

As shown in Figure 6, the driving circuit 13, is constituted by a transistor 72 to whose base is fed the alarm signal passed by the AND circuit 71 when the alarm set signal is high level. The emitter of the transistor 72 is grounded and its collector is connected to one side of the speaker 14, the other side of which is connected with a supply terminal (not shown) of, for example, +1.5 volts.

Referring now to the operation of the generating circuit 12 of Figure 6, Figure 8 is a timing chart of the respective output signals D_1 to D_8 of the AND circuits 41 to 48 which produce pulses in turn with a time delay of 1/65536 seconds. The AND circuits 41 to 48 decode the output signals Q_0 , $\bar{Q}_0$, Q_1 , $\bar{Q}_1$, Q_2 , $\bar{Q}_2$, Q_3 , $\bar{Q}_3$ from the divider circuit 2.

The output signals D_1 to D_8 are fed to the reset terminal of the flip-flop 70 through the respective transmission gates 51 to 58. For instance the transmission gate 51, when conductive, passes the signal D_1 and resets the flip-flop 70 so at the output of the latter appears a signal having a 1/16 duty cycle and a frequency of 4096Hz and a pulse width of 1/65536 seconds as shown in Figure 9(a). Likewise, when the transmission gate 52 is conductive, the signal D_2 causes the flip-flop 70 to produce at its output a signal of 2/16 duty cycle as shown in Figure 9(b). When the transmission gates 53 to 58 are conductive, the signals D_3 to D_8 are passed and the signals appearing at the output of the flip-flop 70 are as shown in Figures 9(c) to 9(h). Thus the signals combined to form the alarm signal from the flip-flop 70 all have the same frequency, namely 4096Hz, but different duty cycles namely 1/16, 2/16, 3/16, 4/16, 5/16, 6/16, 7/16, 8/16 corresponding to the signals D_1 to D_8 . The transmission gates 51 to 58 are not conductive simultaneously and are controlled respectively by the output signals from the ring counter 80. Since the signal $\bar{Q}_{11}$ is applied to the clock terminal CL of

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the ring counter 80, the output signals Q_A to Q_P from the ring counter 80 lag one another by a time delay of 1/16 seconds, each signal Q_A to Q_P having a frequency of 1Hz as shown by the timing chart of Figure 10.

5 A transmission gate is rendered conductive when its N-channel gate is a high level and its P-channel gate is at a low level. For instance, the N-channel gate of the transmission gate 58 is at a high level when the signal Q_A is at a high level, the signal Q_A being fed to the N-channel gate via the junction point T_8 . The P-channel gate of the transmission gate 58 is at a low level due to the inverter 68, to whose input the signal Q_A is also fed. Thus the transmission gate 58 is conductive and the signal D_8 is passed by the transmission gate 58 so that in that instance the signal at the output of the flip-flop 70 has an 8/16 duty cycle. The transmission gate 57 is conductive when the signal Q_B is at high level so that the flip-flop 70, at that instance, produces a signal with a duty cycle of 7/16. Thus, when the signals Q_C , Q_D , Q_E are at a high level, the transmission gates 56, 55, 54 are conductive respectively and the flip-flop 70 produces signals of 6/16, 5/16, 4/16 duty cycle respectively. The signals Q_F , Q_G are connected to the junction point T_3 via the OR circuit 81, the signals Q_H , Q_I , Q_J are connected to the junction point T_2 via the OR circuit 82 and the signals Q_K , Q_L , Q_M , Q_N , Q_O , Q_P are connected to the junction point T_1 via the OR circuit 83. Therefore, when the outputs of the OR circuits 81, 82, 83 are at a high level, respective transmission gates 53, 52, 51 are conductive and the signals appearing from that instant from the flip-flop 70 have duty cycles of 3/16, 2/16, and 1/16.

Figure 11 shows the waveform of the signals at the junction points T_8 to T_1 , where the junction points T_8 to T_4 receive the signals Q_A to Q_E respectively and are high level for 1/16th of a second. The high level period of the junction point T_3 is 2/16 seconds due to signals Q_F , Q_G , the high level period of the junction point T_2 is 3/16 seconds due to the signals Q_H , Q_I , Q_J and the high level period of the junction point T_1 is 6/16 seconds due to the signals Q_K , Q_L , Q_M , Q_N , Q_O , Q_P . The duty cycle of the alarm signal produced by the flip-flop 70 thus varies as shown in Figure 12. As will be seen, the duty cycle varies from 8/16 to 1/16 with a repeat period of 1 second. Thus the alarm signal from the flip-flop 70 has a varying duty cycle and a frequency of 4096Hz and this alarm signal is fed to the AND circuit 71 which also receives the alarm set signal produced by the coincidence circuit 9. The AND circuit 71 thus passes the alarm signal from the flip-flop 70 only when a predetermined alarm

time coincides with the minutes and hours of the actual time of day.

The driving circuit receives the alarm signal from the generating circuit 12 via the AND circuit 71 and drives the speaker 14. The speaker 14 may be an electro-magnetic speaker of 80Ω coil resistance and 4mH inductance. Figure 15 illustrates the sound pressure obtained by the application of the varying duty cycle alarm signal from the flip-flop 70 to the base of the transistor 72. The supply voltage to the speaker 14 was, in this instance 1.5V and the sound pressure was measured at a distance of 10 centimeters from the speaker, 0dB representing a 0.002 microbar. Since the transistor 72 receives the alarm signal from the flip-flop 70 when the AND circuit 71 is conductive, the conducting period of the transistor 72 is different according to the duty cycle of the alarm signal (the high level period of the signal fed to the base of the transistor 72) and therefore the sound pressure obtained by variation of current flow in the transistor 72 through the speaker 14 is as shown in Figure 15. As mentioned above, the alarm signal from the flip-flop 70 has a varying duty cycle as shown in Figure 12 and when the alarm set signal is at a high level and the transistor 72 receives the alarm signal from the flip-flop 70, the variation with time of the sound pressure produced by the speaker 14 is as shown in Figure 16. Although Figure 16 shows a stepped variation in sound pressure, the actual sound is like the ringing of bells and attenuation of the sound appears to be smooth. This is because the human ear cannot sensitively react to abrupt sound pressure variation during such a short period. As illustrated, the variation of the duty cycle of the audible signal produced by the speaker 14 effects the variation of sound pressure and a sound similar to a ringing of bells can be obtained. It will be appreciated that various sounds can be obtained by variation of the construction of the generating circuit 12.

Figure 13 illustrates a modification of the generating circuit 12 of Figure 6. In this embodiment the ring counter 80 still has 16 steps but its clock terminal CL receives the signal $\bar{Q}_8$ (frequency 128Hz) from the flip-flop stage 28 of the divider circuit 2 (Figure 5). The signal Q_A from the ring counter 80 is fed to the junction point T_4 , the signal Q_B is fed to the junction point T_8 , the signals Q_C , Q_D , Q_E , Q_F are fed to an OR circuit 91, the output of which is fed to the junction point T_8 , and the signals Q_G , Q_H are fed to an OR circuit 92 whose output is connected to the junction point T_7 . The signal Q_I is fed to the junction point T_6 , the signal Q_J is fed to the junction point T_5 , the signal Q_K is fed to the junction point T_4 , the signal Q_L is fed to the

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junction point T_3 , the signals Q_M , Q_N , Q_O , are fed to an OR circuit 93 whose output is connected to the junction point T_2 and the signal Q_P is connected to the junction point T_3 . The other parts of the generating circuit, not shown in Figure 13, are as shown in Figure 6, and this embodiment operates in a similar manner. The output signals Q_A to Q_P from the ring counter 80 are similar to those shown in Figure 10, but since the signal fed to the clock terminal CL of the ring counter 80 has a frequency of 128Hz, the period of each of the output signals Q_A to Q_P is 1/8 seconds and the high level period is 1/128 seconds. Accordingly, the junctions T_4 , T_5 , T_6 , T_7 become high level respectively for 1/128 seconds, 1/128 seconds, 4/128 seconds and 2/128 seconds in turn, and the junction points T_8 , T_9 , T_{10} , T_{11} become high level for 1/128 seconds, the junction point T_{12} becomes high level for 3/128 seconds and the junction point T_{13} becomes high level for 1/128 seconds in turn. When the junction points T_2 to T_8 are at a high level, the signals, which when combined produce the alarm signal, have a frequency of 4096Hz and duty cycles which are respectively 2/16, 3/16, 4/16, 5/16, 6/16, 7/16, 8/16. Figure 14 illustrates the form of the alarm signal from the flip-flop 70. The sound pressure obtained when the speaker 14 is driven by the alarm signal of Figure 14 is shown in Figure 17.

Though the variation of sound pressure is also stepped as shown in Figure 17, it appears to the human ear to be smooth. Moreover, since the period of the sound pressure variation in this embodiment is 1/8 seconds, i.e. quicker than in the embodiment of Figure 6, a tremolo effect is obtained.

The two embodiments of the present invention illustrated above produce a comfortable and impressive alarm sound compared with the conventional monotonous and uncomfortable alarm sound. It is to be understood that the invention is not limited to the embodiments illustrated, but that other variations of the alarm sound are possible. Namely, by variation of the arrangement of duty cycle (Figures 12 and 14), variation of grading of the duty cycle (8 steps from 1/16 to 8/16 in the present embodiment) and variation in the number of steps of the ring counter 80 and frequency of the signal applied to the clock terminal CL thereof (16Hz and 128Hz by 16 steps in the present embodiment), various alarm sounds can be obtained.

The highest frequency existing within an electronic timepiece, i.e. the frequency of the reference time signal from the oscillator circuit 1, is f_0 (for example, 32,768Hz in this embodiment) and if the frequency of the audible sound is f_A (4096Hz in this

embodiment) the duty cycle is, at a minimum, $f_A/2.f_0$ (1/16 in this embodiment). For instance if the frequency of the audible sound is 2048Hz, the duty cycle may be based on 1/32 and smoother variation of sound pressure is possible. Whilst the frequency of the audible sound is set at 4096Hz in the present embodiments of the invention, an alarm sound of different tone may be obtained by selective combination of various duty cycles available.

The illustrated embodiments of the present invention eliminate the defects of conventional alarm electronic timepieces, namely, monotonous, mechanical and artificial alarm sounds caused by rectangular waveform signals, by producing a smooth amplitude variation of the sound pressure. Further, it is possible to generate a natural sound such as the ringing of bells or a tremolo effect. Although the above is a psychological effect and is rather subjective, the practical effects are great. Namely, according to the present invention, analog circuits such as D—A transducers, analog signal amplifiers and the like are not necessary to provide analog variation of the sound pressure and so an alarm electronic timepiece according to the present invention can be composed of digital circuit elements, so that the circuit construction is relatively simple. An alarm electronic timepiece according to the present invention can be easily made of MOS integrated circuit construction as used in most electronic wrist watches at present.

Further, various different alarm sounds can be produced for different purposes. For instance, in an alarm electronic timepiece having a plurality of channels, a different alarm sound can be produced in each of the channels. Especially, due to the miniaturization of the circuitry of electronic timepieces, an alarm electronic timepiece can not only be provided with time display functions but also with an audible information function.

As an example of the various different alarm sounds that can be produced by the alarm generating circuit 12, one possibility is where the alarm signal decreases in amplitude with time so that the volume of the alarm sound gradually decreases.

WHAT WE CLAIM IS:

1. An alarm electronic timepiece comprising: time keeping means for producing timing signals; a display device connected to receive the timing signals and to display an actual time of day; alarm setting means for memorising a predetermined alarm time and for producing an alarm set signal when the alarm time and the actual time of day

junction point T_3 , the signals Q_M , Q_N , Q_O , are fed to an OR circuit 93 whose output is connected to the junction point T_2 and the signal Q_P is connected to the junction point T_3 . The other parts of the generating circuit, not shown in Figure 13, are as shown in Figure 6, and this embodiment operates in a similar manner. The output signals Q_A to Q_P from the ring counter 80 are similar to those shown in Figure 10, but since the signal fed to the clock terminal CL of the ring counter 80 has a frequency of 128Hz, the period of each of the output signals Q_A to Q_P is 1/8 seconds and the high level period is 1/128 seconds. Accordingly, the junctions T_4 , T_6 , T_8 , T_7 become high level respectively for 1/128 seconds, 1/128 seconds, 4/128 seconds and 2/128 seconds in turn, and the junction points T_6 , T_5 , T_4 , T_3 become high level for 1/128 seconds, the junction point T_2 becomes high level for 3/128 seconds and the junction point T_1 becomes high level for 1/128 seconds in turn. When the junction points T_2 to T_8 are at a high level, the signals, which when combined produce the alarm signal, have a frequency of 4096Hz and duty cycles which are respectively 2/16, 3/16, 4/16, 5/16, 6/16, 7/16, 8/16. Figure 14 illustrates the form of the alarm signal from the flip-flop 70. The sound pressure obtained when the speaker 14 is driven by the alarm signal of Figure 14 is shown in Figure 17.

Though the variation of sound pressure is also stepped as shown in Figure 17, it appears to the human ear to be smooth. Moreover, since the period of the sound pressure variation in this embodiment is 1/8 seconds, i.e. quicker than in the embodiment of Figure 6, a tremolo effect is obtained.

The two embodiments of the present invention illustrated above produce a comfortable and impressive alarm sound compared with the conventional monotonous and uncomfortable alarm sound. It is to be understood that the invention is not limited to the embodiments illustrated, but that other variations of the alarm sound are possible. Namely, by variation of the arrangement of duty cycle (Figures 12 and 14), variation of grading of the duty cycle (8 steps from 1/16 to 8/16 in the present embodiment) and variation in the number of steps of the ring counter 80 and frequency of the signal applied to the clock terminal CL thereof (16Hz and 128Hz by 16 steps in the present embodiment), various alarm sounds can be obtained.

The highest frequency existing within an electronic timepiece, i.e. the frequency of the reference time signal from the oscillator circuit 1, is f_0 (for example, 32,768Hz in this embodiment) and if the frequency of the audible sound is f_A (4096Hz in this

embodiment) the duty cycle is, at a minimum, $f_A/2.f_0$ (1/16 in this embodiment). For instance if the frequency of the audible sound is 2048Hz, the duty cycle may be based on 1/32 and smoother variation of sound pressure is possible. Whilst the frequency of the audible sound is set at 4096Hz in the present embodiments of the invention, an alarm sound of different tone may be obtained by selective combination of various duty cycles available.

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Further, various different alarm sounds can be produced for different purposes. For instance, in an alarm electronic timepiece having a plurality of channels, a different alarm sound can be produced in each of the channels. Especially, due to the miniaturization of the circuitry of electronic timepieces, an alarm electronic timepiece can not only be provided with time display functions but also with an audible information function.

As an example of the various different alarm sounds that can be produced by the alarm generating circuit 12, one possibility is where the alarm signal decreases in amplitude with time so that the volume of the alarm sound gradually decreases.

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1. An alarm electronic timepiece comprising: time keeping means for producing timing signals; a display device connected to receive the timing signals and to display an actual time of day; alarm setting means for memorising a predetermined alarm time and for producing an alarm set signal when the alarm time and the actual time of day



coincide; audible warning means which is rendered operative by the alarm set signal; and alarm signal generating means including first means for producing a plurality of audio frequency signals having different duty cycles and second means for combining the audio frequency signals to produce an alarm signal whose amplitude varies with time and which causes the audible warning means, when operative, to produce an audible warning.

2. A timepiece as claimed in claim 1 in which the time keeping means includes an oscillator circuit for generating a standard time signal.

3. A timepiece as claimed in claim 2 in which the arrangement is such that, when the standard time signal has a frequency f_0 and the audio frequency signals each have the same frequency f_A , the minimum duty cycle of the audio frequency signals is $f_A/2f_0$.

4. A timepiece as claimed in claim 2 or 3 in which the time keeping means includes a frequency divider circuit having a plurality of divider stages for frequency dividing the standard time signal, the generating means being connected to receive a plurality of

signals of different frequencies from the divider circuit and to produce the audio frequency signals therefrom.

5. A timepiece as claimed in any preceding claim in which the generating means is such that the alarm signal decreases in amplitude with time.

6. A timepiece as claimed in any preceding claim in which the second means is arranged to produce a cyclically amplitude varying alarm signal.

7. A timepiece as claimed in claim 6 in which the second means includes a ring counter whose rate of counting is controlled, in operation, by a signal from the time keeping means.

8. An alarm electronic timepiece substantially as herein-described with reference to and as shown in Figures 4 to 17 of the accompanying drawings.

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