

## WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a source structure penetrated by a first penetrating  
5 portion;

a first stack structure disposed on the source structure and  
penetrated by a second penetrating portion overlapping the first  
penetrating portion;

a second stack structure disposed on the first stack  
10 structure and extending to overlap the first penetrating portion  
and the second penetrating portion; ~~and~~

channel pillars passing through the second stack structure  
and the first stack structure; and

a slit passing through the first stack structure and the  
15 second stack structure and crossing one side of the second  
penetrating portion,

wherein the slit does not overlap the first penetrating  
portion.

20 2. The semiconductor device of claim 1, wherein the  
second penetrating portion is wider than the first penetrating  
portion.

3. The semiconductor device of claim 1, wherein the

second penetrating portion includes a center region overlapping the first penetrating portion and an edge region extending from the center region and overlapping the source structure.

5           4. The semiconductor device of claim 1, further comprising an insulating pattern filling the first penetrating portion and the second penetrating portion and having a T-shaped cross-sectional structure.

10           5. The semiconductor device of claim 1, ~~further comprising a slit traversing~~ wherein the slit traverses a space between the channel pillars to pass through the first stack structure and the second stack structure, ~~and extending to cross one side of the second penetrating portion.~~

15           6. The semiconductor device of claim 5, wherein the slit includes an end portion facing the first penetrating portion,

              wherein an edge of the source structure defined by the first penetrating portion protrudes further towards a center of  
20           the second penetrating portion than an edge of the first stack structure defined by the second penetrating portion in a horizontal direction, and

              wherein the end portion of the slit overlaps a portion of the source structure protruding further than the first stack structure.

7. The semiconductor device of claim 1, wherein the source structure includes at least one doped semiconductor layer completely penetrated by the first penetrating portion.

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8. The semiconductor device of claim 7, wherein the source structure further includes an insulating layer formed on the at least one doped semiconductor layer and an etch stop layer formed on the insulating layer.

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9. The semiconductor device of claim 8, wherein the etch stop layer includes a silicon layer.

10. The semiconductor device of claim 1, wherein the first  
15 stack structure includes a first region penetrated by the channel pillars and second regions extending from the first region to be disposed at opposite sides of the second penetrating portion, and

wherein the second stack structure includes a dummy stack  
20 structure overlapping the second penetrating portion and a gate stack structure extending to overlap the first region and the second region.

11. The semiconductor device of claim 10, wherein each of

the first stack structure and the gate stack structure includes interlayer insulating layers and conductive patterns alternately stacked, and

wherein the dummy stack structure includes dummy interlayer insulating layers extending from the interlayer insulating layers of the gate stack structure in a horizontal direction and sacrificial insulating layers disposed between the dummy interlayer insulating layers.

12. The semiconductor device of claim 10, further comprising:

a contact plug passing through the dummy stack structure to extend into the second penetrating portion and the first penetrating portion; and

a peripheral circuit structure disposed under the source structure and the contact plug and coupled to the contact plug.

13. The semiconductor device of claim 1, further comprising supporting structures passing through a portion of the first stack structure adjacent to the second penetrating portion and extending to pass through the second stack structure,

wherein the supporting structures include at least one of insulating pillars, an insulating bar extending further than each

of the insulating pillars in a horizontal direction, and dummy channel pillars having a same structure as the channel pillars.

14. A semiconductor device, comprising:

5 a source structure penetrated by a first penetrating portion;

a first stack structure disposed on the source structure and divided into memory blocks by first slits; ~~and~~

10 a second penetrating portion passing through the first stack structure of each of the memory blocks and overlapping the first penetrating portion, ~~—~~; and

a second slit passing through the first stack structure and crossing one side of the second penetrating portion,

wherein the second slit does not overlap the first penetrating portion, and

15 wherein the source structure includes a protruding portion protruding further towards a center region of the second penetrating portion than an edge of the first stack structure defined by the second penetrating portion in a horizontal  
20 direction.

15. The semiconductor device of claim 14, further comprising:

a second stack structure disposed on the first stack

structure and extending to overlap the first penetrating portion;  
and

channel pillars passing through the second stack structure  
and the first stack structure.

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16. The semiconductor device of claim 15, ~~further~~  
~~comprising a second slit traversing~~ wherein the second slit  
traverses a space between the channel pillars to pass through

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the first stack structure and the second stack structure between  
the first slits neighboring each other, ~~and crossing one side of~~  
~~the second penetrating portion,~~

~~wherein the second slit does not overlap the first~~  
~~penetrating portion.~~

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17. The semiconductor device of claim 16, wherein the  
second slit includes an end portion facing the first penetrating  
portion, and

wherein the end portion of the second slit overlaps the  
protruding portion of the source structure.

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18. The semiconductor device of claim 16, wherein the  
second stack structure includes a gate stack structure extending  
from the second silt towards the first slits to overlap the first  
stack structure, and a dummy stack structure extending from

the gate stack structure to overlap the first penetrating portion,  
wherein the gate stack structure and the first stack  
structure include interlayer insulating layers and conductive  
patterns alternately stacked, and

5 wherein the dummy stack structure includes dummy  
interlayer insulating layers extending from the interlayer  
insulating layers of the gate stack structure to overlap the first  
penetrating portion, and sacrificial insulating layers disposed  
between the dummy interlayer insulating layers.

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19. The semiconductor device of claim 15, further  
comprising:

an insulating pattern filling the first penetrating portion  
and the second penetrating portion;

15 a contact plug passing through the insulating pattern and  
the second stack structure on the insulating pattern; and

a peripheral circuit structure disposed under the source  
structure and the contact plug and coupled to the contact plug.

20 20. The semiconductor device of claim 15, further  
comprising supporting structures passing through a portion of  
the first stack structure adjacent to the second penetrating  
portion and extending to pass through the second stack  
structure,

wherein the supporting structures include at least one of insulating pillars, an insulating bar extending longer than each of the insulating pillars in a horizontal direction, and dummy channel pillars having a same structure as the channel pillars.

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21. The semiconductor device of claim 14, wherein the source structure includes at least one doped semiconductor layer completely penetrated by the first penetrating portion.

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22. A semiconductor device, comprising:

a source structure including an etch stop layer and penetrated by a first penetrating portion; ~~and~~

a first stack structure disposed on the source structure and penetrated by a second penetrating portion overlapping the first penetrating portion; ~~and~~ and

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a slit passing through the first stack structure and crossing one side of the second penetrating portion,

wherein the slit does not overlap the first penetrating portion, and

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wherein the second penetrating portion is wider than the first penetrating portion.

~~23. A method of manufacturing a semiconductor device, the method comprising:~~

~~forming a first stack structure by alternately stacking first and second material layers on a source stack structure;~~

~~forming a first penetrating portion passing through the first stack structure and the source stack structure; and~~

5 ~~forming a second penetrating portion exposing a top surface of the source stack structure by etching the first stack structure from a side portion of the first penetrating portion~~

10 ~~24. The method of claim 23, wherein the forming of the second penetrating portion comprises:~~

~~forming first grooves by selectively etching the second material layers exposed through a side portion of the first penetrating portion; and~~

15 ~~removing the first grooves by selectively etching the first material layers exposed through the side portion of the first penetrating portion.~~

~~25. The method of claim 23, further comprising:~~

20 ~~forming an insulating pattern filling the first and second penetrating portions; and~~

~~forming a second stack structure by alternately stacking third and fourth material layers on the insulating pattern and the first stack structure.~~

~~26. The method of claim 25, further comprising forming supporting structures passing through the first stack structure adjacent to the second penetrating portion and extending to pass through the second stack structure.~~

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~~27. The method of claim 25, further comprising forming channel pillars passing through the first stack structure and the second stack structure and extending into the source stack structure.~~

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~~28. The method of claim 27, further comprising forming a slit traversing a space between the channel pillars to pass through the first stack structure and the second stack structure, and crossing one side of the second penetrating portion.~~

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~~29. The method of claim 28, wherein the slit does not overlap the first penetrating portion.~~

~~30. The method of claim 28, wherein an end portion of the slit facing the first penetrating portion overlaps the source stack structure exposed by the second penetrating portion.~~

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~~31. The method of claim 27, further comprising forming first slits and a second slit passing through the first stack~~

~~structure and the second stack structure,~~

~~wherein the first slits divide each of the first stack structure and the second stack structure into memory blocks, and~~

~~wherein the second slit traverses a space between the channel pillars to pass through each of the memory blocks and crosses a portion of the second penetrating portion.~~

~~32. The method of claim 31, further comprising:~~

~~forming gate regions exposing the channel pillars by removing the second material layers of the first stack structure and the fourth material layers of the second stack structure through the first slits and the second slit; and~~

~~filling the gate regions with conductive patterns.~~

~~33. The method of claim 32, wherein the forming of the gate regions is controlled such that the fourth material layers overlapping the first penetrating portion remain as dummy layers.~~

~~34. The method of claim 25, wherein each of the first material layers and the third material layers includes a silicon oxide layer, and~~

~~wherein each of the second material layers and the fourth~~

~~material layers includes a silicon nitride layer.~~

5      ~~35. The method of claim 25, further comprising forming a contact plug passing through the insulating pattern and the second stack structure on the insulating pattern.~~

10      ~~36. The method of claim 35, wherein the contact plug is coupled to a peripheral circuit structure disposed under the source stack structure.~~

~~37. The method of claim 23, wherein the source stack structure includes at least one doped semiconductor layer.~~