



Abstract

**A METHOD AND APPARATUS FOR CONTROLLING
GROUND BOUNCE**

The present invention is directed to a method of diminishing ground
5 bounce in integrated circuits (300). Two separate techniques are used
simultaneously to diminish the problem of ground bounce. First, impedance (470,
480) is placed between a power source bus (340) on the integrated circuit and an
external power source (310); and between a ground bus (330) on the chip and an
external ground (310). This effectively dampens ground bounce oscillations in the
10 power and ground leads of the chip. Secondly, capacitance is dynamically added to
the pre-drive of an output buffer (510) with a capacitance node. Dynamic digital
sizing is utilized in both techniques and therefore both techniques are responsive to
the changing performance variations within the chip.

This Sheet Has Been Replaced

