CLAIMS

What is claimed is:

1. A device comprising:

a packaging substrate having a top surface and a bottom surface:

a hybridized device having a bottom surface on the top surface of the packaging substrate, the hybridized device comprising:

a silicon backplane comprising a plurality of input/output (I/O) pins, each of the plurality of I/O pins corresponding to one of a plurality of digital interfaces or one of a plurality of external power supplies, and

a light-emitting diode (LED) array having a bottom surface on a top surface of the silicon backpack;

a plurality of passive components on the top surface of the packaging substrate, the plurality of passive components comprising at least one de-coupling capacitor corresponding to each of the plurality of external power supplies, at least one resistor for setting an LED current, and a crystal for setting a frequency for at least one of the plurality of digital interfaces; and

a plurality of conductive connectors electrically coupled between the top surface of the hybridized device and the top surface of the packaging substrate.

2. The device of claim 1, wherein the plurality of passive components are within 10 mm of at least one of the plurality of I/O pins.

3. The device of claim 1, wherein the hybridized device is on a central region of the top surface of the packaging substrate and the plurality of passive components surround the hybridized device on the top surface of the packaging substrate.

4. The device of claim 1, wherein the LED array is a monolithic array comprising 20,000 or more plurality of light-emitting segments spaced 20 μm or less apart.

5. The device of claim 1, wherein the packaging substrate is a multiple layer circuit board.

6. The device of claim 5, wherein a top layer of the multiple layer circuit board comprises the plurality of passive components and an analog ground, and a layer of the multiple layer circuit board below the top layer comprises a digital ground plane.

7. The device of claim 6, wherein another layer of the multiple layer circuit board below the top layer comprises control signal routing.

8. The device of claim 5, wherein a bottom layer of the multiple layer circuit board comprises a plurality of conductive pads, at least some of the plurality of conductive pads being electrically coupled to a respective one of the plurality of passive components by a through-circuit board connector.

9. The device claim 5, further comprising a metal member embedded in the packaging substrate, extending through all layers of the multiple layer circuit board, and having a top surface thermally coupled to a bottom surface of the hybridized device.

10. A device comprising:

a hybridized device comprising:

a silicon backplane comprising a plurality of input/output (I/O) pins, and

a light-emitting diode (LED) array having a bottom surface on a top surface of the silicon backplane; and

a packaging substrate, a bottom surface of the hybridized device being on a top surface of the packaging substrate, the packaging substrate comprising:

a plurality of passive components on the top surface,

a plurality of contacts on the top surface, and

a plurality of conductive connectors electrically coupled between the I/O pins and the plurality of contacts,

at least a first group of the plurality of contacts corresponding to an external LED power supply, a second group of the plurality of contacts corresponding to an external analog power supply, and a third group of the plurality of contacts corresponding to an external digital power supply.

11. The device of claim 10, wherein a first group of the plurality of passive components for the first external power supply is adjacent the first group of the plurality of contacts and a second group of the plurality of passive components for the second external power supply is adjacent the second group of the plurality of contacts.

12. The device of claim 10, wherein a third group of the plurality of passive components for the third external power supply is adjacent the third group of the plurality of contacts.

13. A device comprising:

a control board having a plurality of top contacts on a top surface of the control board; and

a light-emitting device package comprising:

a hybridized device on a top surface of a packaging substrate, the hybridized device comprising a plurality of input/output (I/O) pins each corresponding to one of a plurality of digital interfaces to the control board or one of a plurality of external power supplies on the control board,

a plurality of bottom contacts on a bottom surface of the packaging substrate,

a plurality of passive components on the top surface of the packaging substrate, the plurality of passive components including at least one de-coupling capacitor corresponding to each of the plurality of external power supplies, at least one resistor for setting an LED current, and a crystal for setting a frequency for at least one of the plurality of digital interfaces,

a plurality of vias electrically coupled between the plurality of passive components on the top surface of the packaging substrate and the plurality of bottom contacts on the bottom surface of the packaging substrate, and

a plurality of conductive connectors electrically coupled between a top surface of the hybridized device and the top surface of the packaging substrate,

the light-emitting device package mounted on the control board with the bottom contacts on the light-emitting device package electrically coupled to the top contacts on the control board.

14. The device of claim 13, wherein the hybridized device comprises a silicon backplane and a monolithic array on the silicon backplane, the monolithic array comprising 20,000 or more plurality of light-emitting segments spaced 20 µm or less apart.

15. The device of claim 14, wherein the packaging substrate is a multiple layer circuit board having a first layer comprising the plurality of passive components and an analog ground, a second layer comprising control signal routing between the silicon backplane and the control board, and a third layer comprising a digital ground plane.