

A CIRCUIT FOR REDUCING ALIASING NOISE

Field of the Invention

5 This invention relates to an electronic circuit that reduces aliasing noise and particularly to an electronic circuit that reduces aliasing noise on a colour video image on a colour cathode ray tube display.

Background of the Invention

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 In colour video monitors a cathode ray tube (CRT) is commonly used to display a colour image. As is known, a predetermined number of picture elements or pixels on the screen of the CRT light up to produce the displayed image. Each pixel is made up of a triad of coloured phosphor deposits i.e. red, green and blue, which light up when hit by an electron beam. Located immediately behind the screen is a plate, commonly referred to as a shadow mask, which has a hole associated with each of the pixels on the screen. Three scanning electron beams, designated red, green and blue, pass through the holes and hit the corresponding coloured phosphor deposits on the screen. The shadow mask ensures that the electron beams, for e.g. the red beam, passes through the holes and hits only the red phosphor deposits on the screen. To simplify further description, only the red beam and the red phosphor deposits will be referred to, however, the description that follows applies equally to the green and blue electron beams and corresponding phosphor deposits.

20 The arrangement of the triads of phosphor deposits on the screen are such that the phosphor deposits form rows. Consequently, the red phosphor deposits located in even numbered rows are horizontally displaced by a predetermined distance from the red phosphor deposits located in odd numbered rows. In monitors having small screen sizes, say 35.56 centimetres or less, the horizontal displacement between the red phosphor deposits in the odd and even rows does not produce visible defects on the displayed image. However, when the size of the screen is 43.18 centimetres or more, the horizontal displacement between the phosphors deposits in the odd and even rows result in dark horizontal lines on the displayed image. The dark lines are caused by the red electron beam hitting areas on the shadow mask between the holes instead of

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passing through the holes when the even numbered rows are scanned, and is referred to as aliasing noise.

Hence, to reduce aliasing noise the horizontal position of the scan of the red electron beam across the even numbered rows of phosphor deposits must be shifted horizontally by the predetermined distance, in order for the red electron beam to pass through the holes in the shadow mask and hit the red phosphor deposits in the even numbered rows.

One method of shifting the position of the scan of the red electron beam is disclosed by SGS-Thomson in the operation of their integrated circuit part no. TDA9105. In this circuit, a horizontal synchronising signal, which controls the timing of the horizontal scan of the red electron beam, is used to switch a reference voltage between two levels. One level when the red electron beam scans the odd numbered rows of phosphor deposits and another level when it scans the even numbered rows. The level of the reference voltage determines the horizontal position of a horizontal scan of the red electron beam on the screen. Hence, switching the reference voltage between the two levels at the same frequency as the horizontal synchronising signal shifts the position of the horizontal scan of the even numbered rows of phosphor deposits, relative to the position of the horizontal scan of the odd numbered rows.

Disadvantages of this method are the need for additional circuitry and an additional output pin for coupling to additional external circuitry when the circuit is packaged in an IC. Another disadvantage is, as the horizontal synchronising signal controls the timing of the horizontal scans and also provides the timing for the switching of the reference voltage, conflicts between the two timing functions can cause erratic positioning of the horizontal scan. In addition, because the stability of the horizontal scan of the electron beam is dependent on the stability of the reference voltage, switching the reference voltage between two levels affects the stability of the horizontal scan of the red electron beam, and can cause visible defects on the displayed image.

Brief Summary of the Invention

The present invention therefore seeks to provide a circuit that reduces aliasing noise in images on CRT displays having relatively large screens, reduces the need for additional circuitry and additional output pins

when the circuit is packaged in an integrated circuit, and will less adversely affect the stability of the horizontal scan of the electron beam across the screen of the CRT.

Accordingly, in one aspect the invention provides a circuit for a cathode ray tube (CRT) display comprising: a control circuit having a first input coupled to receive a horizontal synchronising signal and a second input coupled to receive a switching reference signal, and a first output that outputs a square pulse signal and a second output that outputs a horizontal drive signal having horizontal CRT drive pulses; and a multiplexer having a control input coupled to the first output of the control circuit, a first input coupled to receive a first reference level signal, a second input coupled to receive a second reference level signal, which second reference level signal is different from the first reference level signal, and an output coupled to the second input of the control circuit that outputs the switching reference signal.

In another aspect the invention provides a circuit for a cathode ray tube (CRT) display comprising: a control circuit means having a first input for receiving a horizontal synchronising signal and a second input for receiving a switching reference signal, and a first output for providing a square pulse signal and a second output for providing a horizontal drive signal having horizontal CRT drive pulses; and a multiplexer means having a control input coupled to the first output of the control circuit means for receiving the square pulse signal, a first input for receiving a first reference level signal, a second input for receiving a second reference level signal, which second reference level signal is different from the first reference level signal, and an output coupled to the second input of the control circuit means for providing the switching reference signal.

Brief Description of the Drawings

An embodiment of the invention will now be more fully described, by way of example, with reference to the drawings, of which:

FIG. 1 shows a schematic a prior art horizontal position control system coupled to a CRT;

FIGS. 2A and 2B show timing diagrams of the horizontal position control system in FIG. 1;

FIG. 3 shows coloured phosphors on a portion of the screen of the CRT in FIG. 1;

FIG. 4 shows aliasing noise on the portion of the screen in FIG. 3;

FIGS. 5A and 5B show parts of a video signal that causes the aliasing noise in FIG. 4;

FIG. 6 shows the portion of the screen in FIG. 3 with aliasing noise reduced;

FIG. 7A and 7B show video signals that reduce aliasing noise in FIG. 6;

FIG. 8 shows a schematic of the horizontal position control system in FIG. 1 with a prior art aliasing noise reducing circuit;

FIGS. 9A, 9B and 9C show timing diagrams of the aliasing noise reducing circuit in FIG. 8;

FIG. 10 shows a schematic of a horizontal position control system with an aliasing noise reducing circuit in accordance with the present invention;

FIG. 11 shows a block diagram of the aliasing noise reducing circuit in FIG. 10;

FIG. 12 shows a block diagram of the horizontal position control system with the aliasing noise reducing circuit in FIG. 10; and

FIG. 13A-13K shows timing diagrams of the horizontal position control system with the aliasing noise reducing circuit in FIG. 10.

Detailed Description of the Drawings

FIGS. 1, 2A and 2B illustrate a horizontal position control system which is coupled to receive a horizontal synchronising signal (HSYNC) from an input 5, and coupled to provide a horizontal drive output signal (HORIZONTAL DRIVE OUTPUT) 215 to a deflection circuit 8 of a cathode ray tube (CRT) 15. A plate or shadow mask 20 is located in the CRT 15 behind a screen 30. Horizontal synchronising pulses 220 (only one shown) on the horizontal synchronising signal (HSYNC) 200 and the horizontal position control system 10 control the generation of horizontal drive pulses 246 (only one shown) on the horizontal drive output signal (HORIZONTAL DRIVE OUTPUT) 215. Each horizontal drive pulse 246 causes electron beams (not shown) in the CRT 15 to scan horizontally across the screen 30.

An external capacitor 25 is coupled between the horizontal position control system 10 and an electrical reference potential or electrical ground. A voltage (PD2) on the external capacitor 25 relative to the electrical ground, sets the time the horizontal drive pulses 26 are generated by the horizontal position control system 10 which also sets the position of the horizontal position of the horizontal scans of the electron beams across the screen 30. Hence, varying the voltage on the external capacitor (PD2) 25 varies the horizontal position of the horizontal scans of the electron beams across the screen 30.

FIG. 3 illustrates circular coloured phosphor deposits arranged in rows on a portion of the internal surface of the screen 30. The letters R, G and B on the phosphor deposits indicate the colour red, green and blue respectively, that is given off by the phosphor deposits when they are hit by correspondingly designated red, green and blue electron beams. An set of three, or triad, of adjacent red, green and blue coloured phosphor deposits constitute a picture element or pixel 33.

FIG. 4 illustrates the phosphor deposits on the portion of the screen 30 with the red phosphor deposits 40 identified with an R. The following description will only refer to the red phosphor deposits 40 and the corresponding red electron beam. However, it should be understood that the following description applies equally to the green and blue phosphor deposits and the corresponding green and blue electron beams.

The rows of phosphor deposits arranged from the top to the bottom of the screen 30 can be sequentially numbered, and divided into odd and even numbered rows. The first and third row of the phosphor deposits on the portion of the screen 30 will be referred to as odd numbered rows 31 and the middle row will be referred to as an even numbered row 32. From the arrangement of the phosphor deposits on the screen 30, it can be seen that the red phosphor deposits 40 in the even numbered row 32 are horizontally displaced from the red phosphor deposits 40 in the odd numbered rows 31.

FIGS. 5A and 5B show a video signal 48 which is provided to the CRT 15 to control the intensity of the red electron beam (not shown) as it is directed across the screen 30. The video signal 48 has a video data part 50 which controls the intensity of the red electron beam as it is scanned across the odd numbered rows 31, and an even video data part 60 which controls the intensity of the red electron beam as it is scanned across the even

numbered row 32. Pulses 55 and 66 indicate the time when the intensity of the red electron beam is increased to hit the red phosphor deposits 40 on the screen. It should be understood that the video signal 48 is a continuous signal and that the separation of the video signal 48 into parts 50 and 60 is for illustration purposes only.

The pulses 55 of the odd video data part 50 occur when the scanning red electron beam is directed at the red phosphor deposits 40. Hence, the intensity of the red electron beam is increased when it is directed at the red phosphor deposits 40 on the odd numbered rows 31. This causes the red electron beam to hit the red phosphor deposits 40, as indicated by the squares 45, which give off red light on the screen 30.

However, pulses 65 of the even video data part 60 do occur when the scanning red electron beam is directed at the red phosphor deposits 40 on the even numbered row 32. Consequently, the red electron beam does not hit the red phosphor deposits 40, and instead, hits the areas between the holes on the shadow mask 20, as indicated by the squares 52. This results in unlighted red phosphor deposits 40 on the screen 30 and is known as aliasing noise.

In FIGS. 6, 7A and 7B the phosphor deposits on the portion of the screen 30 and the video signal 48 are shown, however, the even video data part 60 is separated from the odd video data part 50 by a predetermined time 64. This displacement synchronises the time the pulses 65 occur with the time the red electron beam is directed at the red phosphor deposits 40 on the even numbered rows 32. Consequently, the red electron beam hits the red phosphor deposits 40 on the even numbered rows 32 as indicated by squares 70. Therefore, to reduce aliasing noise, the position of the horizontal scan of the even numbered rows 32 must to be displaced horizontally from the position of the horizontal scan of the odd numbered rows 31 by a predetermined distance. This displacement translates into a predetermined time delay 64.

FIGS. 8 illustrates the horizontal position control system 10 coupled to a prior art aliasing noise reducing circuit 105. As before, the horizontal position control system 10 is coupled to the input 5 and the deflection circuit 8 of the CRT 15. In addition, the aliasing noise reducing circuit 105 includes a modulator 110 which is coupled to receive a horizontal synchronising signal (HSYNC) (200 in FIG. 9A) from the input 5 and provide a switching signal to a buffer 115. The buffer 115 provides a buffered switching signal

to an output which is coupled to resistors 120 and 125 that are coupled in series, and free end of the resistor 125 is coupled to an electrical reference potential or ground. The external capacitor 25 is coupled between the horizontal position control system 10 and the junction of the two resistors
 5 120 and 125.

FIGS. 9A, 9B and 9C illustrate the timing diagrams for the horizontal position control system 10 with the aliasing noise reducing circuit 105, and their operation will now be described with reference to FIGS. 5 and 6. The horizontal position control system 10 receives a horizontal synchronising
 10 signal (HSYNC) 200 having a horizontal synchronising pulse 220 from the input 5. In response to receiving the horizontal synchronising pulse 220, the horizontal position control system 10 generates a ramp signal (HRAMP) 210. The horizontal position control system 10 compares the voltage (PD2) 205 on the external capacitor 25 with the ramp signal (HRAMP) 210, and
 15 generates the horizontal drive signal (HORIZONTAL DRIVE OUTPUT) 215 with the horizontal drive pulse 246 when the voltage of the ramp signal (HRAMP) 210 reaches the voltage (PD2) 205.

Changing the voltage (PD2) 205 from a lower level 222 to a higher level 232 causes a change in the time when the horizontal drive pulse 246
 20 is generated from an earlier time 244 to a later time 248. This changes the position of a horizontal scan on the screen 30. The prior art aliasing reducing circuit 105 uses the horizontal synchronising pulse 220 of the horizontal synchronising signal 200 to switch the voltage (PD2) 205 between the two levels 222 and 232. The first level is used when the red
 25 electron beam is scanning the odd numbered rows of phosphor deposits (31 in FIG. 4), and the second level when the red electron beam is scanning the even numbered rows of phosphor deposits (32 in FIG. 4). Changing or shifting the position of the horizontal scan changes the time the pulses (65 in FIG. 5) of the even video data part (60 in FIG. 5) occurs to
 30 synchronise with the time when the red electron beam is directed at the red phosphor deposits (40 in FIG. 5) on the even numbered rows (32 in FIG. 4).

Typically, the time the horizontal drive pulse 246 is generated is very close to the time when the horizontal synchronising pulse 220 occurs. The difference in time being determined primarily by the time delay of the
 35 deflection circuit 8. Hence, because the aliasing noise reducing circuit 105 uses the horizontal synchronising pulses 220 to switch the voltage (PD2) 205 from the lower level 222 to the higher level 232, the voltage of the ramp

signal (HRAMP) 210 can become equal to the voltage (PD2) 205 at any one of several levels 228, 230 or 224. This causes the horizontal drive pulse 246 to be generated either at an earlier time 244 or at a later time 248, depending on when the voltage (PD2) 205 switches between the two levels 222 and 232, and at which point the voltage of the ramp signal (HRAMP) 210 becomes equal to the voltage (PD2) 205.

The present invention advantageously employs a switching signal that is derived from a horizontal position control system that switches between the two levels at a time which does not coincide with the occurrence of the horizontal synchronising pulse 220. Thus, substantially reducing the erratic generation of the horizontal drive pulse 246.

FIG. 10 illustrates a horizontal synchronising circuit 300 coupled to an aliasing noise reducing circuit 302 in accordance with the present invention. The horizontal synchronising circuit 300 is coupled to receive a horizontal synchronising signal (HSYNC) (200 in FIG. 13A) from the input 5, and coupled to provide a horizontal drive output signal (HORIZONTAL DRIVE OUTPUT) (525 in FIG. 13K) to the deflection circuit 8 of the CRT 15. The external capacitor 25 is coupled between the horizontal synchronising circuit 300 and an electrical reference potential or ground. The aliasing noise reducing circuit 302 is coupled to receive a square pulse signal (H1PULSE) (507 in FIG. 13B) from the horizontal synchronising circuit 300, and coupled to provide a switching reference signal (DAC OUTPUT) (511 in FIG. 13D) to the horizontal synchronising circuit 300.

The horizontal synchronising circuit 300 receives the horizontal synchronising signal (HSYNC) (200 in FIG. 13A) and derives the square pulse signal (H1PULSE) (507 in FIG. 13B) from the horizontal synchronising signal (HSYNC) (200 in FIG. 13A). The horizontal synchronising circuit 300 then provides the square pulse signal (H1PULSE) (507 in FIG. 13B) to the aliasing noise reducing circuit 302 which generates and provides the switching reference signal (DAC OUTPUT) (511 in FIG. 13D) back to the horizontal synchronising circuit 300. The horizontal synchronising circuit 300 uses the switching reference signal (DAC OUTPUT) (511 in FIG. 13D) to switch the position of the odd and even numbered horizontal scans of the red electron beam in the CRT 15, to displace the position of the even numbered scans from the position of the odd numbered scans.

FIG. 11 illustrates a block diagram of the aliasing noise reducing circuit 302 which is coupled to provide the switching reference signal (DAC OUTPUT) (511 in FIG. 13D) to a first and second ramp generator 340 and 345 in the horizontal position control circuit 300. The broken line separates the blocks of the aliasing noise reduction circuit 302 from the blocks of the horizontal position control circuit 300. The aliasing noise reducing circuit 302 includes a toggle flip-flop or bistable multivibrator 320 which is coupled to receive the square pulse signal (H1PULSE) (507 in FIG. 13B) from the horizontal synchronising circuit 300. The toggle flip-flop 320 has an output which is coupled to provide a modulation signal (MODULATION PULSE) (509 in FIG. 13C) having half the frequency of the square pulse signal (H1PULSE) (507 in FIG. 13B).

A latch 330 stores a digital displacement value which corresponds with a desired displacement between the positions of the even and odd numbered horizontal scans on the screen 30. A multiplexer 325 has a first input that is coupled to the output of the toggle flip-flop 320 to receive the modulation signal (MODULATION PULSE) (509 in FIG. 13C), and a second input coupled to the latch 330 to retrieve the digital displacement value therefrom. A third input of the multiplexer 325 is coupled to electrical ground to provide a digital reference value. Dependent on the state of the modulation signal (MODULATION PULSE) (509 in FIG. 13C), either the digital displacement value or the digital reference value is provided from an output of the multiplexer 325.

A digital to analogue converter (DAC) 335 is coupled to the output of the multiplexer 325 and provides the switching reference signal (DAC OUTPUT) (511 in FIG. 13D) having a higher analogue reference level (HIGHER REFERENCE VOLTAGE LEVEL) (530 in FIG. 13D) when the digital displacement value is selected and retrieved by the multiplexer 325; and having a lower analogue reference level (LOWER REFERENCE VOLTAGE LEVEL) (540 in FIG. 13D) when the digital reference value is selected by the multiplexer 325.

The first ramp generator 340 has an input which is coupled to receive the switching reference signal (DAC OUTPUT) (511 in FIG. 13D). When the switching reference signal (DAC OUTPUT) (511 in FIG. 13D) has the lower analogue reference level (LOWER REFERENCE VOLTAGE LEVEL) (540 in FIG. 13D) the first ramp generator 340 generates a lower ramp voltage (545 in FIG. 13E) i.e. a voltage ramp that starts at the lower

analogue reference level. When the switching reference signal (DAC OUTPUT) (511 in FIG. 13D) has the higher analogue reference level (HIGHER REFERENCE VOLTAGE LEVEL) (530 in FIG. 13D) the first ramp generator 340 generates a higher ramp voltage (535 in FIG. 13E) i.e. a voltage ramp that starts at the higher analogue reference level (HIGHER REFERENCE VOLTAGE LEVEL) (530 in FIG. 13D). The operation of the second ramp generator 345 is similar to that of the first ramp generator 340 and will be described in detail later.

With reference to FIGS. 12 and 13A-K a reference phase detector 405 has a first input which is coupled to the input 5 to receive the horizontal synchronising signal (HSYNC) 200 from a controller (not shown). A second input of the reference phase detector 405 is coupled to receive a roll over signal from a first output of a 5-bit counter-decoder 420. The reference phase detector 405 provides an output signal indicative of the phase difference between the horizontal synchronising signal (HSYNC) 200 and the roll over signal to an input of a loop filter 410.

The reference phase detector 405 is a comparator which is enabled by the horizontal synchronising pulse 220 of the horizontal synchronising signal (HSYNC) 200 to charge or discharge the loop filter 410. When the horizontal synchronising signal (HSYNC) 200 is a logic 1, no current is sunk from or sourced to the input of the loop filter 410 by the reference phase detector 405. When the roll over signal from the first output of the 5-bit counter-decoder 420 is a logic 1 and the horizontal synchronising signal (HSYNC) 200 is a logic 0 i.e. when the horizontal synchronising pulse 220 occurs, current is sunk to the output of the reference phase detector 405 from the input of the loop filter 410. When the roll over signal from the first output of the 5-bit counter-decoder 420 is a logic 0, and the horizontal synchronising signal (HSYNC) 200 is a logic 0 i.e. when a horizontal synchronising pulse 220 does occur, current is sourced from the output of the reference phase detector 405 to the input of the loop filter 410.

When a phase locked loop formed by the reference phase detector 405, the loop filter 410, an oscillator 415 and the 5-bit counter-decoder 420, is in a locked condition, the rising edge of the roll over signal from the first output of the 5-bit counter-decoder 420, which is the most significant bit of the 5-bit counter-decoder 420, is synchronised with the centre of the horizontal synchronising pulse 220. In addition, when the phase locked loop is in the locked condition the charging and discharging time of the

loop filter 410 are equal. The loop filter 410 includes a 2.7K resistor, a 1uF capacitor and a 10nF capacitor.

5 The loop filter 410 has an output coupled to provide a filtered output signal voltage to an input of the oscillator 415. The oscillator 415 is a voltage controlled oscillator which has an input coupled to receive the filtered output signal from the output of the loop filter 410, and has an output to provide a square pulse output signal (CLK). The frequency of the square pulse output signal (CLK) is inversely proportional to the filtered output voltage of the loop filter 410. The output of the oscillator 115 is coupled to provide the square pulse output signal (CLK) to an input of the 5-bit counter-decoder 420. In addition, another output of the oscillator 415 is coupled to provide a reference signal (IREF) to the first ramp generator 340 and to the second ramp generator 345. The reference signal (IREF) provides a timing reference which ensures synchronisation between these three circuits.

15 The 5-bit counter-decoder 420 is a synchronous 5-bit up counter 418 and a decoder 422. The 5-bit up counter 418 is a roll over counter which is coupled to receive the pulses of the square pulse output signal (CLK) from the output of the oscillator 415, count the pulses of the square pulse output signal (CLK), and maintain a current count value (CNTR1) of the number of pulses that are counted. The current count value (CNTR1) of the 5-bit up counter 418 ranges from 00(hex) to 1F(hex) after which the 5-bit up counter 418 rolls over to 00(hex) and repeats the count sequence.

25 The decoder 422 has an input which is coupled to an output of the 5-bit up counter 418. The decoder 422 has a first output coupled to provide the roll over signal via the first output of the 5-bit counter decoder 420 to the second input of the reference phase detector 405. The decoder 422 has a second output coupled to an input of the first ramp generator 340. The decoder 422 functions as a first digital comparator and provides a first reference output signal from the second output to the first ramp generator 340. The first reference output signal is a square pulse signal (H1PULSE) 507. When the first ramp generator 340 receives the square pulse signal (H1PULSE) 507, the first ramp generator 340 generates a first ramp output signal (HRAMP1) 515 having a higher ramp voltage 535 or a lower ramp voltage 545. The square pulse signal (H1PULSE) has a start time 607 and a stop time 609 determined by a predetermined count value of the 5-bit up counter 418. Hence, by selecting a lower predetermined count value the

generation of the higher ramp voltage 535 or the lower ramp voltage 545 by the first ramp generator 340 can be advanced, i.e. made to occur earlier in time.

Alternatively, by selecting a higher predetermined count value the generation of the higher ramp voltage 535 or the lower ramp voltage 545 can be retarded, i.e. made to occur later in time. When the predetermined count value is 1D(hex), and the current count value (CNTR1) counted by the 5-bit up counter 418 is 1D(hex), indicating the start time 607, the square pulse signal (H1PULSE) 507 changes state from a logic 0 to a logic 1. In addition, when the current count value (CNTR1) counted by the 5-bit up counter 418 is 0D(hex) indicating the stop time 609, the square pulse signal (H1PULSE) 507 changes state from a logic 1 to a logic 0. The selection of the start time 607 and the stop time 609 of the square pulse signal (H1PULSE) 507 may be dependent on design considerations such as the input drive requirements of the first ramp generator 340. In another embodiment, the selection of the start time 607 and the stop time 609 may be programmable variables and can therefore be dynamically set and stored.

Hence, the phase locked loop formed by the reference phase detector 405, the loop filter 410, the oscillator 415 and the 5-bit counter-decoder 420, function as a synchronised pulse generator.

In addition, the 5-bit counter decoder 420 generates additional output signals which include a current count signal from the 5-bit counter 418 via a third output, and a load signal from the decoder 422 via a fourth output. The current count signal indicates the current count value (CNTR1) of the 5-bit up counter 418. The load signal provides an indication to the horizontal drive output pulse width counter 424 to load the contents of a latch 426 into the horizontal drive output pulse width counter 424.

The aliasing noise reducing circuit 302 has an input which is coupled to receive the square pulse signal (H1PULSE) 507 and provide the switching reference signal (DAC OUTPUT) 511 having either the higher analogue reference level (HIGHER REFERENCE VOLTAGE LEVEL) 530 or the lower analogue reference level (LOWER REFERENCE VOLTAGE LEVEL) 540 to the first and second ramp generators 340 and 345.

The first ramp generator 340 has an input which is coupled to receive the square pulse signal (H1PULSE) 507 from the second output of the decoder 422, and an output which is coupled to a first input of the first

comparator 428. When the square pulse signal (H1PULSE) 507 is a logic 1, a capacitor in the first ramp generator 340 is charged by a current source, in the first ramp generator 340, to generate the higher ramp voltage 535 or the lower ramp voltage 545. And, when the square pulse signal (H1PULSE) 507 is a logic 0, the capacitor in the first ramp generator 340 is discharged by another current source in the first ramp generator 340, to generate a decreasing ramp voltage 537.

The first ramp generator 340 also has an input for receiving the switching reference signal (DAC OUTPUT) 511 from the aliasing noise reducing circuit 302. When the switching reference signal (DAC OUTPUT) 511 has a lower analogue reference level (LOWER REFERENCE VOLTAGE LEVEL) 540 and the square pulse signal (H1PULSE) 507 is received, the first ramp generator 340 generates the lower ramp voltage 545. When the switching reference signal (DAC OUTPUT) 511 has a higher analogue reference level (HIGHER REFERENCE VOLTAGE LEVEL) 530 and the square pulse signal (H1PULSE) 507 is received, the first ramp generator 340 generates the higher ramp voltage 535. A broken line superimposes the lower analogue reference level (LOWER REFERENCE VOLTAGE LEVEL) 540 and the lower ramp voltage 545 over the higher analogue reference level (HIGHER REFERENCE VOLTAGE LEVEL) 530 and the higher ramp voltage 535 to show the differences therebetween.

Note that irrespective of whether the first ramp generator 340 generates the higher ramp voltage 535 or the lower ramp voltage 545, the voltage level of the decreasing ramp voltage 537 remains substantially the same.

A clamping circuit is implemented in the first ramp generator 340 to limit the voltage of the first ramp output signal (HRAMP1) 515 between 1 volt and 6 volts. The higher ramp voltage 535 and the lower ramp voltage 545 each span a time range or duration which must accommodate both, the propagation delay compensation range of the external deflection circuit 8 of the CRT 15, and a horizontal position adjustment range of a video image on the screen 30 of the CRT 15.

The first comparator 428 compares the voltage of the higher ramp voltage 535 or the lower ramp voltage 545 of the first ramp output signal (HRAMP1) 515 and the voltage of a horizontal position signal (HORIZONTAL POSITION) 513 to produce a flyback reference signal (FLYBACK REF) 517. Depending on whether the higher ramp voltage 535

or the lower ramp voltage 545 of the first ramp output signal (HRAMP1) 515 is provided by the first ramp generator 340, the flyback reference signal (FLYBACK REF) 517 has an earlier rising edge 546 or a later rising edge 548. The phase detector 432 receives and compares the flyback reference signal (FLYBACK REF) 517 and a flyback pulse 553 of a current flyback signal (FLYBACK) 519 to provide an output signal to the external capacitor 25 which produces an output voltage (PD2) 521.

The voltage level of the output voltage (PD2) 521 is indicative of the phase difference between the rising edge 546 or 548 of the flyback reference signal (FLYBACK REF) 517 and the flyback pulse 553 of the current flyback signal (FLYBACK) 519. The output voltage (PD2) 521 is provided to a first input of a second comparator 442.

A second digital comparator 434 has a first input coupled to the third output of the decoder 422 to receive the current count signal from the 5-bit up counter 418. The second digital comparator 434 has a second input coupled to receive a selected count signal from an output of an up-down counter 438. The selected count signal indicates a selected count value (CNTR2) of the up-down counter 438.

The second digital comparator 434 compares the current count value (CNTR1) indicated by the current count signal, and the selected count value (CNTR2) indicated by the selected count signal, and provides a second reference output signal from an output to an input of the second ramp generator 345. When the current count value (CNTR1) and the selected count value (CNTR2) are the same, the second digital comparator 434 generates a second reference output signal (H2PULSE). The second reference output signal is a square pulse (H2PULSE) that changes from a logic 0 to a logic 1 when the selected count value (CNTR2) is 19(hex) at start time 611. The square pulse (H2PULSE) changes from a logic 1 to a logic 0 when the selected count value (CNTR2) is 09(hex) at stop time 612. The selected count value (CNTR2) determines the time when the second comparator 140 generates the square pulse signal (H2PULSE).

The square pulse signal (H2PULSE) is provided from the output of the second digital comparator 434 to an input of the second ramp generator 345 causing the second ramp generator 345 to generate a second ramp signal (HRAMP2) 523. The second ramp generator 345 also has an input for receiving the switching reference signal (DAC OUTPUT) 511 from the aliasing noise reducing circuit 302. When the switching reference signal

(DAC OUTPUT) 511 has the higher analogue reference level (HIGHER REFERENCE VOLTAGE LEVEL) 530 and the square pulse signal (H2PULSE) is received, the second ramp generator 345 generates a higher ramp voltage 575. When the switching reference signal (DAC OUTPUT) 511 has the lower analogue reference level (LOWER REFERENCE VOLTAGE LEVEL) 540 and the square pulse signal (H2PULSE) is received, the second ramp generator 345 generates a lower ramp voltage 561.

The second ramp generator 345 is similar to the first ramp generator 340, however, a capacitor having a smaller value is used. When the square pulse signal (H2PULSE) is a logic 1, the capacitor in the second ramp generator 345 is charged by a current source in the second ramp generator 345 to generate the higher ramp voltage 575 or the lower ramp voltage 545. And, when the square pulse signal (H2PULSE) is a logic 0, the capacitor in the second ramp generator 345 is discharged by another current source in the second ramp generator 345, to generate a decreasing ramp voltage 561. Note that irrespective of whether the second ramp generator 345 generates the higher ramp voltage 575 or the lower ramp voltage 561, the voltage level of the decreasing ramp voltage 577 remains substantially the same. The second ramp signal (HRAMP2) 523 having the higher ramp voltage 575 or the lower ramp voltage 561 is provided to a second input of the second comparator 442.

The selected count value (CNTR2) determines the time when the second comparator 442 generates the square pulse signal (H2PULSE) which causes the second ramp generator 315 to generate the either the higher ramp voltage 575 or the lower ramp voltage 561, depending on whether the switching reference signal (DAC OUTPUT) 511 has the higher analogue reference level (HIGHER REFERENCE VOLTAGE LEVEL) 530 or the lower analogue reference level (LOWER REFERENCE VOLTAGE LEVEL) 540. Hence, by varying the selected count value (CNTR2) the start of the voltage ramp 561 or 575 can be advanced or retarded independently of the start of the higher ramp voltage 545 or the lower ramp voltage 545 of the first ramp output signal (HRAMP1) 515.

The up-down counter 438 is coupled to receive an up input signal (UP), a down input signal (DOWN) and a vertical flyback signal (VERTICAL FLYBACK) from an external source (not shown). The up-down counter 438 comprises a 5-bit counter. The up-down counter 438 counts up when it

receives the up input signal (UP), and it counts down when it receives the down input signal (DOWN), thereby setting the selected count value (CNTR2).

When the up input signal (UP) is a logic 1 and the down input signal (DOWN) is a logic 0, the up-down counter 438 will count up i.e. $CNTR2 = CNTR2 + 1$ when the externally provided vertical flyback signal (VERTICAL FLYBACK) is received. When the up input signal (UP) is a logic 0 and the down input signal (DOWN) is a logic 1, the up-down counter 438 will count down i.e. $CNTR2 = CNTR2 - 1$ when the vertical flyback signal (VERTICAL FLYBACK) is received. When both the up input signal (UP) and the down input signal (DOWN) are a logic 0, the up-down counter 320 will stop counting i.e. $CNTR2 = CNTR2$ when the vertical flyback signal (VERTICAL FLYBACK) is received.

An upper limit comparator 436 has a first input coupled to the external capacitor 25 to receive the output voltage (PD2) 521. A second input of the upper limit comparator 436 is coupled to receive a predetermined upper reference voltage signal (V_{up}) from an external source (not shown). The upper limit comparator 436 compares the voltage level of the output voltage (PD2) 521 with the voltage level of the predetermined upper reference voltage signal (V_{up}) and produces the up input signal (UP).

When the voltage level of the output voltage (PD2) 521 is higher than the voltage level of the predetermined upper reference voltage signal (V_{up}), the upper limit comparator 436 generates the up input signal (UP) having a logic 1. When the voltage level of the output voltage (PD2) 521 is lower than the voltage level of the predetermined upper reference voltage signal (V_{up}), the upper limit comparator 436 generates the up input signal (UP) having a logic 0.

A lower limit comparator 440 has a first input coupled to the external capacitor 25 to receive the output voltage (PD2) 521. A second input of the lower limit comparator 440 is coupled to receive a predetermined lower reference voltage signal (V_{down}) from an external source (not shown). The lower limit comparator 440 compares the voltage level of the output voltage (PD2) 521 and the voltage level of the predetermined lower reference voltage signal (V_{down}), and produces the down input signal (DOWN).

When the voltage level of the output voltage (PD2) 521 is lower than the voltage level of the predetermined lower reference voltage signal

(Vdown), the lower limit comparator 440 generates the down input signal (DOWN) having a logic 1. When the voltage level of the output voltage (PD2) 521 is higher than the voltage level of the predetermined lower reference voltage signal (Vdown), the lower limit comparator 440 generates the down input signal (DOWN) having a logic 0.

The second comparator 442 compares the output voltage (PD2) 521 which is provided to the first input of the second comparator 442, and the second ramp signal (HRAMP2) 523 having the higher ramp voltage 575 or the lower ramp voltage 561 which is provided to the second input of the second comparator 442. The second comparator 442 has an output which is coupled to a rising/falling edge decoder 444 and generates a logic output signal (COMP2) which has a rising edge and a falling edge.

The second comparator 442 generates the rising edge on the logic output signal (COMP2) when the voltage of the second ramp signal (HRAMP2) 523 is greater than the output voltage (PD2) 521, and the second comparator 442 generates the falling edge on the logic output signal (COMP2) when the voltage of the second ramp signal (HRAMP2) 523 is less than the voltage level of the output voltage (PD2) 521.

When the ramp voltage of the second ramp signal (HRAMP2) 523 is the higher ramp voltage 575, the rising edge of the output signal (COMP2) occurs earlier because the higher ramp voltage 575 ramps up to the level of the output voltage (PD2) 521 in a shorter time than when the ramp voltage of the second ramp signal (HRAMP2) 523 is the lower ramp voltage 561. Conversely, when the ramp voltage of the second ramp signal (HRAMP2) 523 is the lower ramp voltage 561, the rising edge of the output signal (COMP2) occurs later because the lower ramp voltage 561 takes a longer time to ramp up to the level of the output voltage (PD2) 521.

The rising-falling edge decoder 444 is a logic gate that is coupled to receive the logic output signal (COMP2) from the output of the second comparator 442, and coupled to receive a pulse width signal (HWOUTPUT) from an output of the horizontal drive output pulse width counter 424. The rising-falling edge decoder 444 generates an output logic pulse signal (HDRIVE) having a logic output pulse.

The rising edge of the logic output pulse of the output logic pulse signal (HDRIVE) is aligned with the rising edge of the logic output signal (COMP2). The falling edge of the logic output pulse of the output logic pulse signal (HDRIVE) is determined by the falling edge of the pulse width

signal (HWOUTPUT) from the horizontal drive output pulse width counter 424. Hence, the pulse width signal (HWOUTPUT) from the horizontal drive output pulse width counter 424 determines the duty cycle of the logic output pulse of the output logic pulse signal (HDRIVE).

5 An input of the horizontal driver 446 is coupled to the output of the rising-falling edge decoder 444 to receive the logic output pulse of the output logic pulse signal (HDRIVE). In response, the horizontal driver 446 provides a horizontal drive output signal (HORIZONTAL DRIVE OUTPUT) 525 to the deflection circuit 8 of the CRT 15. Upon receiving the horizontal
10 drive output signal (HORIZONTAL DRIVE OUTPUT) 525, the deflection circuit 8 produces the flyback pulse 553 of the flyback signal (FLYBACK) 519.

 When the second ramp signal (HRAMP2) 523 is the higher ramp voltage 575, the rising edge of the output signal (COMP2) and the rising
15 edge of the logic output pulse of the output logic pulse signal (HDRIVE) occurs at an earlier time. Consequently, an earlier rising edge 585 of the horizontal drive output signal (HORIZONTAL DRIVE OUTPUT) 525 is produced. Alternatively, when the second ramp signal (HRAMP2) 523 is the lower ramp voltage 561, the rising edge of the output signal (COMP2) and
20 the rising edge of the logic output pulse of the output logic pulse signal (HDRIVE) occur at a later time. Consequently, a later rising edge 586 of the horizontal drive output signal (HORIZONTAL DRIVE OUTPUT) 525 is produced. In addition, a falling edge 588 of the horizontal drive output signal (HORIZONTAL DRIVE OUTPUT) 525 is determined by the falling
25 edge of the logic output pulse of the output logic pulse signal (HDRIVE).

 The latch 426 has an input coupled to receive a duty cycle control signal (DUTY CYCLE CONTROL) from an external source (not shown), and has an output coupled to an input of the horizontal drive output pulse width counter 424. The duty cycle control signal (DUTY CYCLE CONTROL)
30 conveys data to the latch 426, and the data is then stored in the latch 426. The horizontal drive output pulse width counter 424 is coupled to receive a data input signal from the latch 426, the pulses of the square pulse output signal (CLK) from the output of the oscillator 415, and the load signal (LOAD) from the 5-bit counter decoder 420.

35 The horizontal drive output pulse width counter 424 has an output coupled to an input of the rising/falling edge decoder 444 to provide the pulse width signal (HWOUTPUT). The horizontal drive output pulse width

counter 424 is a down counter having a count value (CNTR3). When the horizontal drive output pulse width counter 424 receives the load signal (LOAD) from the fourth output of the 5-bit counter-decoder 420, the horizontal drive output pulse width counter 424 is triggered to read the stored data from the latch 426.

The stored data in the latch 426 is transmitted by the data input signal to the horizontal drive output pulse width counter 424. For example, when the data read from the latch 426 is 10(hex), then the count value (CNTR3) of the horizontal drive output pulse width counter 424 becomes 10(hex) after loading. Clocked by the pulses of the square pulse output signal (CLK), the horizontal drive output pulse width counter 424 counts down from 10(hex) until the count value (CNTR3) is 00(hex) and then stops counting.

When the horizontal drive output pulse width counter 424 receives the logic output signal (COMP2) from the second comparator 442 the horizontal drive output width counter 424 starts counting down. At the same time, the horizontal drive output pulse width counter 424 causes the output logic pulse signal (HDRIVE) to change from a logic 0 to a logic 1, which causes the horizontal drive output signal (HORIZONTAL DRIVE OUTPUT) 525 to change from a logic 0 to a logic 1, forming the earlier rising edge 585.

When the horizontal drive output pulse width counter 424 is counting down the pulse width signal (HWOUTPUT) remains set to a logic 1. When the horizontal drive output pulse width counter 424 stops counting, the pulse width signal (HWOUTPUT) changes from a logic 1 to a logic 0. This causes the horizontal drive output signal (HORIZONTAL DRIVE OUTPUT) 525 to change from a logic 1 to a logic 0, forming the falling edge 588. Thus, in this way the duty cycle of the horizontal drive output signal (HORIZONTAL DRIVE OUTPUT) 525 is digitally set by the data provide from the latch 426.

A variable gain control 430 is a logic switch to turn ON and OFF a current source. When a vertical pulse of the vertical flyback signal (VERTICAL FLYBACK) is received, the current source is enabled to supply more current to the phase detector 432 to increase its gain, thereby improving the lock time of the phase detector 432.

Further, the first and second ramp generators 340 and 345 each have an additional input for receiving the switching reference signal (DAC

OUTPUT) 511 from the aliasing noise reducing circuit 302. When the first ramp generator 340, receives the switching reference signal (DAC OUTPUT) 511 having the lower analogue reference level (LOWER REFERENCE VOLTAGE LEVEL) 540 it generates the ramp voltage 545, and when the first ramp generator 340, receives the switching reference signal (DAC OUTPUT) 511 having the higher analogue reference level (HIGHER REFERENCE VOLTAGE LEVEL) 530, it generates the ramp voltage 535, which is higher than the ramp voltage 545.

When the higher ramp voltage 545 is compared with the voltage of the horizontal position signal (HORIZONTAL POSITION) 51, the flyback reference signal (FLYBACK REF) 517 is produced having a rising edge 546 and a falling edge 549. As the ramp voltage 535 is higher than the ramp voltage 545, the ramp voltage 535 reaches the level of the horizontal position signal (HORIZONTAL POSITION) 513 in a shorter time than the ramp voltage 545. Consequently, the rising edge 546 occurs earlier than when the switching reference signal (DAC OUTPUT) 511 has the lower analogue reference signal (LOWER REFERENCE VOLTAGE LEVEL). Hence, there is a predetermined time difference 550 between the rising edge 546 when the switching reference signal (DAC OUTPUT) 511 has the higher analogue reference level (HIGHER REFERENCE VOLTAGE LEVEL) 530, and the rising edge 548 when the switching reference signal (DAC OUTPUT) 511 has the lower analogue reference level (LOWER REFERENCE VOLTAGE LEVEL) 540.

When the second ramp generator 345, receives the switching reference signal (DAC OUTPUT) 511 having the lower analogue reference level (LOWER REFERENCE VOLTAGE LEVEL) 540 it generates the ramp voltage 561, and when the second ramp generator 345 receives the switching reference signal (DAC OUTPUT) 511 having the higher analogue reference level (HIGHER REFERENCE VOLTAGE LEVEL) 530, it generates the ramp voltage 575, which is higher than the ramp voltage 561.

When the higher ramp voltage 575 is compared with the output voltage (PD2) 521, the horizontal drive output signal (HORIZONTAL DRIVE OUTPUT) 525 is produced having the earlier rising edge 585, or the later rising edge 586, and a falling edge 588, which is determined by the combination of the rising/falling edge decoder 444 and the horizontal drive output pulse width counter described earlier. As the ramp voltage 575 is

higher than the ramp voltage 561, the ramp voltage 575 reaches the level of the output voltage (PD2) 521 in a shorter time than the ramp voltage 561.

Therefore, the earlier rising edge 585 is produced when the switching reference signal (DAC OUTPUT) 511 has the higher analogue reference level (HIGHER REFERENCE VOLTAGE LEVEL) 530, and the later rising edge 586 is produced when the switching reference signal (DAC OUTPUT) 511 has the lower analogue reference level (LOWER REFERENCE VOLTAGE LEVEL) 540. A time 587 is the time shift between the earlier rising edge 585 and the later rising edge 586. The time shift 587 results in a flyback pulse 553 which is correspondingly shifted in time, and this causes a horizontal shift in the position of the horizontal scan.

Using the switching reference signal (DAC OUTPUT) 511 to only time shift the ramp voltage of the second ramp generator 345, without a similar time shift of the ramp voltage of the first ramp generator, can also achieve the same shift in the horizontal position of horizontal scans of the electron beam. However, the time shift 587 will cause the flyback pulse 553 to be shifted in time, which in turn causes a phase error between the flyback pulse 553 and the rising edge 548 of the unshifted flyback reference signal 517. The horizontal synchronising circuit 300 will attempt to reduce this phase error, and consequently, the level of the output voltage (PD2) 521 will change. Changing the level of the output voltage (PD2) 521, as explained earlier, introduces noise into the horizontal synchronising circuit 300, which is not desirable.

In order to reduce the introduction of noise into the horizontal synchronising circuit 300, the switching reference signal (DAC OUTPUT) 511 is used to shift both the ramp of the first ramp generator 340 and the ramp of the second ramp generator 345, as described above. With this arrangement, both the flyback pulse 553 and the rising edge of the flyback reference signal 517 are shifted equally in time the same time and no significant phase error results. Consequently, the level of the output voltage (PD2) 521 does not change significantly, and this reduces the introduction of noise into the horizontal synchronising circuit 300.

Hence, the described circuit reduces aliasing noise in images on CRT displays having screen sizes 17 inches or more. In addition, no additional circuitry and additional output pins are required, and adverse effects on the stability of the horizontal scan of the electron beam across the screen of the CRT are minimised.

Claims

1. A circuit for a cathode ray tube (CRT) display comprising:
 - 5 a control circuit having a first input coupled to receive a horizontal synchronising signal and a second input coupled to receive a switching reference signal, and a first output that outputs a square pulse signal and a second output that outputs a horizontal drive signal having horizontal CRT drive pulses; and
 - 10 a multiplexer having a control input coupled to the first output of the control circuit, a first input coupled to receive a first reference level signal, a second input coupled to receive a second reference level signal, which second reference level signal is different from the first reference level signal, and an output coupled to the second input of the control circuit that
 - 15 outputs the switching reference signal.
2. A circuit in accordance with claim 1 wherein the control circuit comprises control circuit means for receiving the horizontal synchronising signal and the switching reference signal and for providing the square pulse signal and the horizontal drive signal having horizontal drive pulses, wherein the timing of the horizontal CRT drive pulses is at least partially dependent upon the switching reference signal.
- 20 3. A circuit in accordance with claim 1 further comprising:
 - 25 a first memory having a first digital value that corresponds to the first reference level signal stored therein; and
 - a digital to analogue converter having a digital input coupled to receive the first digital value and an analogue output that outputs the first
 - 30 reference level signal.
4. A circuit as claimed in claim 3 further comprising:
 - 35 a second memory having a second digital value that corresponds to the second reference level signal stored therein; and



the digital to analogue converter having the digital input coupled to receive the second digital value and the analogue output outputting the second reference level signal.

- 5 5. A circuit as claimed in claim 3 wherein the first memory has an input for receiving the first digital value.
6. A circuit as claimed in claim 5 wherein the second memory has an input for receiving the second digital value.
- 10 7. A circuit as claimed in claim 1 wherein the control circuit further comprises a synchronised pulse generator circuit having an input coupled to receive the horizontal synchronising signal and an output coupled to provide the square pulse signal.
- 15 8. A circuit as claimed in claim 7 wherein the synchronised pulse generator circuit comprises synchronised pulse generator circuit means for receiving the horizontal synchronising signal and for providing the square pulse signal, wherein the timing of the square pulse signal is at least
 - 20 partially dependent upon the horizontal synchronising signal.
 9. A circuit according to claim 8 wherein the synchronised pulse generator circuit means comprises:
 - 25 a reference phase detector for receiving the horizontal synchronising signal and a roll over signal and providing an output signal indicative of the phase difference between them;
 - a loop filter coupled to the reference phase detector for receiving the output signal from the reference phase detector and providing a filtered
 - 30 output signal;
 - an oscillator coupled to the loop filter for receiving the filtered output signal and providing an oscillator output signal having pulses at a frequency proportional to the filtered output signal;
 - a roll over counter coupled to the oscillator for receiving the oscillator
 - 35 output signal and counting the pulses thereof, and providing the roll over signal when the current count reaches a roll over value; and



a first digital comparator coupled to the roll over counter for comparing the current count therein with a predetermined count value and providing the square pulse signal when the two counts are the same.

- 5 10. A circuit as claimed in claim 9 wherein the first digital comparator compares the current count therein with the predetermined count value and provides an intermediate square pulse signal when the two counts are the same, and wherein the synchronised pulse generator circuit means further comprises a frequency divider having an input coupled to the first digital
10 comparator for receiving the intermediate square pulse signal and having an output for providing the square pulse signal.

11. A circuit as claimed in claim 10 wherein the frequency divider comprises a toggle bistable multi-vibrator.

- 15 12. A circuit as claimed in claim 1 further comprising a first analogue reference source for providing the first reference level.

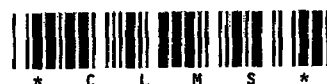
13. A circuit as claimed in claim 1 further comprising a second analogue
20 reference source for providing the second reference level.

14. A monitor having a circuit incorporated therein, the circuit according to any one of the preceding claims.

- 25 15. A circuit for a cathode ray tube (CRT) display comprising:

- a control circuit means having a first input for receiving a horizontal synchronising signal and a second input for receiving a switching reference signal, and a first output for providing a square pulse signal having pulses
30 and a second output for providing a horizontal drive signal having horizontal CRT drive pulses; and

- a multiplexer means having a control input coupled to the first output of the control circuit means for receiving the square pulse signal, a first input for receiving a first reference level signal, a second input for receiving
35 a second reference level signal, which second reference level signal is different from the first reference level signal, and an output coupled to the second input of the control circuit means for providing the switching



reference signal, wherein the timing of the horizontal CRT drive pulses is at least partially dependent upon the switching reference signal.

16. A circuit in accordance with claim 15 further comprising:

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a first memory means for storing a first digital value therein, wherein the first digital value corresponds to the first reference level signal; and

a digital to analogue converting means having a digital input coupled to the first memory means for receiving the first digital value, and
10 an analogue output for providing the first reference level signal.

17. A circuit as claimed in claim 16 further comprising:

a second memory means for storing a second digital value, wherein
15 the second digital value corresponds to the second reference level signal: and

the digital to analogue converting means having the digital input coupled to the second digital memory means for receiving the second digital value, and the analogue output for providing the second reference
20 level signal.

18. A circuit as claimed in claim 15 wherein the control circuit means further comprises a synchronised pulse generator circuit means having an input for receiving the horizontal synchronising signal and an output for
25 providing the square pulse signal, wherein the timing of the pulses of the square pulse signal is at least partially dependent upon the horizontal synchronising signal.

19. A circuit according to claim 18 wherein the synchronised pulse
30 generator circuit means comprises:

a reference phase detector means for receiving the horizontal synchronising signal and a roll over signal and for providing an output signal indicative of the phase difference between them;

35 a loop filter means coupled to the reference phase detector for receiving the output signal from the reference phase detector means and for providing a filtered output signal;



an oscillator means coupled to the loop filter means for receiving the filtered output signal and for providing an oscillator output signal having a series of pulses at a frequency proportional to the filtered output signal;

5 a roll over counter means coupled to the oscillator means for receiving the oscillator output signal and counting the pulses thereof, and for providing the roll over signal when the current count reaches a roll over value; and

10 a first digital comparator means coupled to the roll over counter means for comparing the current count therein with a predetermined count value and for providing the square pulse signal when the two counts are the same.

20. A circuit as claimed in claim 19 wherein the first digital comparator means compares the current count therein with the predetermined count value and provides an intermediate square pulse signal when the two counts are the same, and wherein the synchronised pulse generator circuit means further comprises a frequency divider means having an input coupled to the first digital comparator for receiving an intermediate square pulse signal and having an output for providing the square pulse signal.

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21. A circuit as claimed in claim 20 wherein the frequency divider means comprises a toggle bistable multi-vibrator.

