Abstract

SYSTEM AND APPARATUS FOR WAFER LEVEL INTEGRATION OF COMPONENTS

In a semiconductor package, a substrate has an active surface containing a plurality of active circuits. An adhesive layer is formed over the active surface of the substrate, and a known good unit (KGU) is mounted to the adhesive layer. An interconnect structure electrically connects the KGU and active circuits on the substrate. The interconnect structure includes a wire bond between a contact pad on the substrate and a contact pad on the KGU, a redistribution layer on a back surface of the substrate, opposite the active surface, a through hole via (THV) through the substrate that electrically connects the redistribution layer and wire bond, and solder bumps formed in electrical contact with the redistribution layer. The KGU includes a KGU substrate for supporting the KGU, a semiconductor die disposed over the KGU substrate, and an encapsulant formed over the semiconductor die. (Fig. 3)