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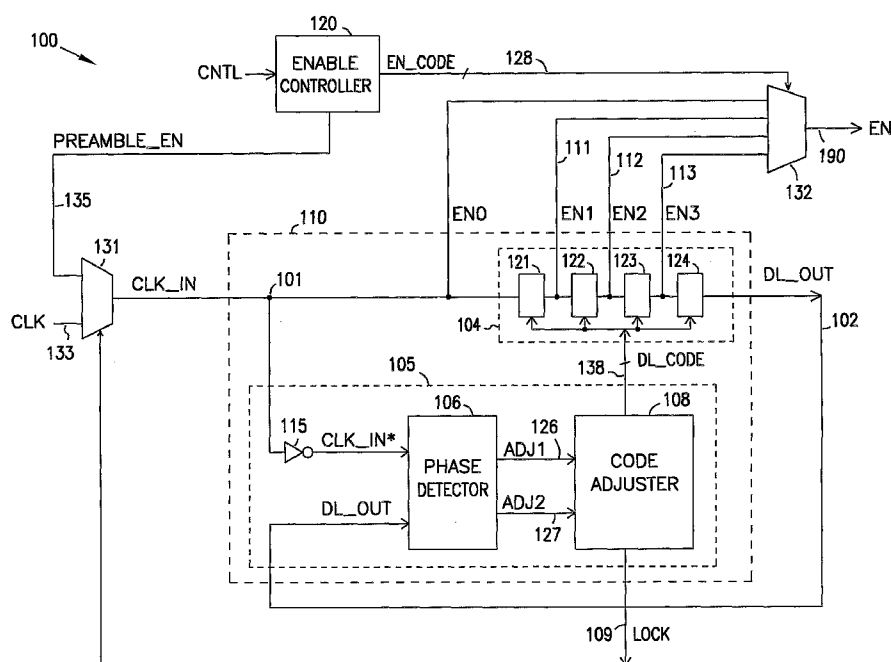
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(54) Title: DIGITAL FREQUENCY LOCKED DELAY LINE



(57) Abstract: A device includes a signal generator having a delay locked circuit for providing a number of output signals based on an input signal. The output signals have a fixed signal relationship with each other and with the input signal. The signal generator also includes a selector for selecting an enable signal from a range of signals formed by the output signals. The device further includes a transceiver circuit in which the transceiver circuit uses the enable signal for data processing.

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