

Apparatus for recording a digital information signal in a track on a record carrier and encoding means for encoding said digital information signal.

The invention relates to an apparatus for recording a digital information signal in a track on a record carrier, the apparatus comprising

- input means for receiving the digital information signal,
- encoding means for encoding the digital information signal so as to obtain a channel signal,
- 5 the encoding means comprising a nT precoder, where n is an integer for which holds $n \geq 1$, and T is the bittime in the digital information signal, the nT precoder comprising signal combination means and delay means for realizing a signal delay of nT ,
- preamble signal generating means for generating a preamble signal,
- switching means for combining the preamble signal and the channel signal, the switching
- 10 means having a first and second input, an output and a control signal input, the first input of the switching means being coupled to an output of the preamble signal generating means,
- timing means for timing the switching means such that the switching means supplies a channel encoded block of information of the digital information signal which is preceded by the preamble signal,
- 15 - writing means for writing the preamble signal and the channel encoded block of information of the digital information signal in the track on the record carrier, and to encoding means for encoding said digital information signal.

An apparatus as defined in the opening paragraph is known from EP-A 492,704, document D1 in the list of related documents that can be found at the end of this

20 description, see especially the figure 12 in document D1. n equals 2 in the prior art apparatus.

The prior art apparatus records a digital information signal, that may be a digital video signal or a digital audio signal or may comprise both the digital video signal

25 and the digital audio signal or may even comprise a digital data signal, in slant tracks on a record carrier. The tracks are formed by a preamble track portion in which a preamble signal is recorded, followed by a data track portion in which the channel signal is recorded. The channel signal recorded in a data track portion is the $2T$ precoded version of a sequence of datablocks (syncblocks) each datablock (syncblock) comprising a sync word which is

followed by a number of bytes of information. The preamble signal is used during reproduction to lock the internal oscillator of the reproducing apparatus to the bitclock included in the preamble signal. Next, the syncwords in the datablocks (syncblocks) are detected so as to enable the retrieval of the data information included in the data blocks.

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The invention aims at improving syncword detection during a subsequent reproduction of the information recorded in the tracks. The apparatus in accordance with the invention is characterized in that the switching means form part of the nT precoder, the second input of the switching means being coupled to an output of the signal combination means, the output of the switching means being coupled to an input of the nT delay means.

The invention is based on the following recognition. The prior art apparatus generates a preamble signal that is defined as a write current pattern. The digital information signal is precoded using the 2T precoder to generate the write current, in order to write the digital information signal on the record carrier. The transition of the preamble signal to the 2T precoded digital information signal during recording results during reproduction in two unknown bits at the start of the reproduced digital information signal. This for the reason that the contents of the 2T delay means in the precoder at the start of precoding the digital information signal is generally not equal to the last two bits of the preamble signal (the write current signal). As a result, two bits less are available during reproduction for syncword detection, as the syncword is the first word in the precoded datastream that directly follows the preamble signal.

In accordance with the invention, the input of the delay means is coupled to the output of the switching means, and thus receives the preamble pattern prior to the switching means switching over to the other position. The contents of the nT delay means is now equal to the last n bits of the preamble signal, and thus are the first n bits of the precoded information defined. This enables the syncword detecting to be more reliable, as an increased number (n) of bits are available for syncword detection. Otherwise said: the syncword detector can detect syncwords that are n bits longer.

Another solution can be applied to the prior art apparatus by advancing the moment of switching over to the other switch position by nT at minimum.

These and other aspects of the invention will be apparent from and further elucidated with reference to embodiments described in the following figure description, in which

figure 1 shows a prior art apparatus,
figure 2 shows an embodiment of a 2T precoder,
figure 3 shows the timing of some signals,
figure 4 shows one solution in accordance with the invention, applied to the
5 apparatus of figure 1,
figure 5 shows an embodiment of an apparatus in accordance with the
invention, using another solution,
figure 6 shows again the timing of some signals in the apparatus of figure 5,
figure 7 shows another embodiment of the apparatus, and
10 figure 8 shows the timing of some signals in the apparatus of figure 7.

Figure 1 shows schematically only the relevant parts of the prior art apparatus. The apparatus forms the recording part of a Partial Response Class IV (PRIV) system. For a further discussion of a PRIV system, reference is made to EP-A 317,013, document D2 in
15 the list of documents. An input terminal 2 is coupled to an input 4 of a 2T precoder 6, an output 8 of which is coupled to a terminal 'a' of a controllable switch 10. A preamble signal generator 12 is present having an output coupled to a terminal 'c' of the switch 10. A terminal b is coupled to an input 16 of a write unit 18. A timing unit 22 is present for generating timing signals for various elements in the apparatus. Figure 1 shows only the
20 generation of a timing signal that is supplied to a control signal input 24 of the switch 10. The write unit 18 is provided with at least one write head for writing the signal applied to its input 16 on a record carrier 20. A 2T precoder is well known in the art. Figure 2 shows an embodiment of a 2T precoder, which comprises a signal combination unit 32 and a delay unit 30.

25 The generator 12 generates a preamble signal in the form of a write current pattern that may comprise a sequence of codewords, as defined in document D1. A codeword could be the following binary sequence

0001110001110000011100011,

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or the inverse binary sequence. The preamble signal is defined as a write current pattern, so that the above sequence is supplied to the write unit 18 directly. That is: without any precoding in a 2T precoder.

The digital information signal is supplied to the input terminal 2 and precoded

in the precoder 6 so as to obtain the write current (the channel signal) for recording the digital information signal on the record carrier 20. Document D1 describes a digital information signal in the form of a sequence of datablocks (syncblocks) each datablock (syncblock) comprising a sync word which is followed by a number of bytes of the digital information. When recording the digital information on the record carrier, first the preamble signal is recorded, followed by the sequence of precoded datablocks. Figure 3 shows in (a) schematically as a function of time the signal supplied to the input 16 of the write unit 20. Under the influence of a timing signal (not shown) generated by timing unit 22, the generator 12 starts at a time instant $t=t_0$ to generate the preamble signal. At this time instant, the switch 10 is in (or: is switched to) the position c-b, so that the preamble signal is supplied to the write unit 18 as a write current and recorded in a track. The generation of the preamble signal is terminated at the time instant $t=t_1$. Next, a source (not shown) starts supplying the digital information signal at time instant $t=t_1$, eg. also under the influence of a timing control signal (not shown) supplied by the timing unit 22. The information signal is 2T precoded and supplied to the a-terminal of the switch 10. Further, under the influence of the a timing control signal supplied by the timing unit 22 to the switch 10, the switch changes its switch position into the position a-b, so that the 2T precoded data is supplied to the write unit 18 at the time instant $t=t_1$. This is shown in (a) of figure 3, which shows the serial datastream (write current) supplied to the write unit 18. (b) in figure 3 shows the timing control signal supplied by the timing unit 22 to the switch 10. Prior to the instant t_1 , the switch is in its position c-b, and after the time instant t_1 , the switch 10 is in its position a-b. As a consequence, the contents of the 2T delay 30 in the precoder 6 at the time instant t_1 is not equal to the last two bits of the preamble signal. This results in problems during reproduction.

(c) in figure 3 shows schematically the signal received upon reproduction. As can be seen, the first two bits b_i, b_{i+1} in the reproduced data are unknown. If the first p bits are defined as a sync word, only $p-2$ bits can be used in a syncword detector to detect the sync word. Such detection is less reliable than if the sync word detector could have made use of all the p bits for sync word detection.

Figure 4 shows a first solution to this problem that can be applied in the apparatus of figure 1. (a) in figure 4 shows the preamble signal generated by the generator 12 in the time interval t_0, t_1 , and the 2T precoded data supplied by the precoder 6 starting at the time instant t_1 . (b) in figure 4 shows the timing signal supplied by the timing unit 22 to the switch 10. As can be seen, the switch 10 switches over to its position a-b two bit periods

T before the time instant t_1 . That means that the last two bits of the preamble signal are not recorded on the record carrier 20. This is not a problem, as the preamble signal is long enough to realize the locking in of the internal oscillator of the reproducing apparatus to the bitclock included in the preamble signal.

5 By switching the switch to the position 2 bit periods before t_1 , this means that at the time instant t_1 , the contents of the 2T delay unit 30 in the precoder 6 is equal to the last two bits of the preamble signal. Starting from the time instant t_1 , precoded data is supplied by the precoder 6 to the write unit 18.

10 Upon reproduction, the datastream shown schematically in (c) of figure 4 is obtained. As can be seen, the bits b_{i-2} , b_{i-1} are unknown. The reproduced data is however valid, starting from the time interval t_1 . As a result, the full p-bit long syncword can be used in the sync detector for syncdetection, during reproduction.

Figure 5 shows another solution of the problem. The apparatus shown in figure 5 shows large resemblances to the apparatus of figure 1. Elements in figure 1, 2 and 5 15 having the same reference numerals are therefore considered to be the same. As can be seen in figure 5, the switch 10 is now incorporated into the 2T precoder 6', in that the b-terminal of the switch 10 is further coupled to the input 50 of the 2T delay unit 30.

(a) in figure 6 shows again the preamble signal generated by the generator 12 in the time interval t_0, t_1 , and the 2T precoded data supplied by the precoder 6'. (b) in figure 6 20 shows the timing signal supplied by the timing unit 22 to the switch 10. As can be seen, the switch 10 switches over to its position a-b at the time instant t_1 . As the input of the 2T delay unit 30 is coupled to the b-terminal of the switch 10, this means that the delay unit 30 is constantly supplied with the preamble signal, so that at the time instant t_1 of switching over, the contents of the delay unit 30 is equal to the last two bits of the preamble signal. As a 25 result, precoded data is supplied by the precoder 6', whilst, moreover, the preamble signal is recorded correctly.

Upon reproduction, the datastream shown schematically in (c) of figure 6 is obtained. As can be seen, all reproduced bits are valid. As a result, the full p-bit long syncword can be used in the sync detector for syncdetection, during reproduction.

30 Figure 7 shows another embodiment, which shows close resemblances with the embodiment of figure 5. A switch 60 is present which multiplexes the preamble signal and the non-precoded data applied to the input 2, under the influence of a timing signal 61 applied to the timing unit 22'. This results in the serial datastream shown in figure 8a. At the time instant t_1 the switch 60 switches over between the positions c-b and a-b. Now the

combination unit 32 in the 2T precoder, as well as the terminal c of the switch 10 receive the serial datastream of figure 8a. At the time instant t_1 the switch 10 switches over from the switch position c-b to the switch position a-b, as can be seen in figure 8b, under the influence of the control signal applied to the input 24. As a result, the signal shown in figure 8c is supplied to the input 16 of the write unit 18.

Various modifications of the invention as explained above are possible. It can more generally be said that an nT precoder could have been used, where n is an integer, for which holds that $n \geq 1$. For the solution described in figure 4, this means that switching over the switch position a-b should take place at the time instant $t_1 - nT$.

Further, for both solutions shown in figure 4 and in the figures 5 and 6, there is no objection in switching over to the switch position a-b earlier than the time instant $t_1 - nT$, provided that the valid portion of the preamble signal after reproduction from the record carrier is long enough to enable a locking in of the internal oscillator of the reproducing apparatus to the bitclock included in the preamble signal.

It should further be noted that the preamble signal and the precoded data as shown in (a) of figure 2 can be recorded as the beginning portion of a track. It is however also possible that a track comprises various track portions serially located in said track. Each track portion may comprise a preamble signal, followed by precoded data. The solutions disclosed above will be applied to the generation of the information so as to generate the track portions in the track.

Further, it should be noted that the combination of the precoder and the switch could have been incorporated into one electronic component, such as an integrated circuit, or could have been realized in software form in a microprocessor.

The recording apparatus in accordance with the invention may be one of the helical scan recording type, or the linear recording type. The invention is equally well applicable in recording apparatuses for recording on disk-like record carriers. Further, the record carrier may be of the magnetic or optical type.

Therefore, it should be observed that the invention is not restricted to the embodiments described, but is limited and defined only by the appended claims.

Related documents

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| (D1) | EP-A 492,704 (PHN 13.546) |
| (D2) | EP-A 317,013 (PHN 12.328) |

CLAIMS

1. Apparatus for recording a digital information signal in a track on a record carrier, the apparatus comprising
- input means for receiving the digital information signal,
 - encoding means for encoding the digital information signal so as to obtain a channel signal,
 - 5 the encoding means comprising a nT precoder, where n is an integer for which holds $n \geq 1$, and T is the bittime in the digital information signal, the nT precoder comprising signal combination means and delay means for realizing a signal delay of nT ,
 - preamble signal generating means for generating a preamble signal,
 - switching means for combining the preamble signal and the channel signal, the switching
 - 10 means having a first and second input, an output and a control signal input, the first input of the switching means being coupled to an output of the preamble signal generating means,
 - timing means for timing the switching means such that the switching means supplies a channel encoded block of information of the digital information signal which is preceded by the preamble signal,
 - 15 - writing means for writing the preamble signal and the channel encoded block of information of the digital information signal in the track on the record carrier,
- characterized in that, the switching means form part of the nT precoder, the second input of the switching means being coupled to an output of the signal combination means, the output of the switching means being coupled to an input of the nT delay means.
- 20 2. Apparatus as claimed in claim 1, characterized in that, the timing means are adapted to supply a control signal to the control signal input of the switching means such that the switching means realize an internal connection between its first input and its output during a time interval coinciding in time with at least a part of a time interval in which the preamble signal generating means generates said preamble signal, and such that the switching
- 25 means realize an internal connection between its second input and its output during a time interval in which said block of information of the digital signal is supplied to the input of the nT precoder for channel encoding.
3. Apparatus as claimed in claim 2, characterized in that the timing means are adapted to supply a control signal to the control signal input of the switching means such that



the switching means switches over from the internal connection between its first input and its output to the internal connection between its second input and its output at a time instant mT prior to the time instant of the start of the supply of said block of information of the digital information signal, where m is an integer for which holds $m \geq 0$.

- 5 4. Apparatus as claimed in claim 3, characterized in that $m=0$.
5. Apparatus for recording a digital information signal in a track on a record carrier, the apparatus comprising
- input means for receiving the digital information signal,
 - encoding means for encoding the digital information signal so as to obtain a channel signal,
 - 10 the encoding means comprising a nT precoder, where n is an integer for which holds $n \geq 1$, and T is the bittime in the digital information signal, the nT precoder comprising signal combination means and delay means for realizing a signal delay of nT ,
 - preamble signal generating means for generating a preamble signal,
 - switching means for combining the preamble signal and the channel signal, the switching
 - 15 means having a first and second input, an output and a control signal input, the first input of the switching means being coupled to an output of the preamble signal generating means,
 - timing means for timing the switching means such that the switching means supplies a channel encoded block of information of the digital information signal which is preceded by the preamble signal,
 - 20 - writing means for writing the preamble signal and the channel encoded block of information of the digital information signal in the track on the record carrier,
- characterized in that, the timing means are adapted to supply a control signal to the control signal input of the switching means such that the switching means realize an internal connection between its first input and its output during a time interval coinciding in time with
- 25 a part of a time interval in which the preamble signal generating means generates said preamble signal, and that the switching means switches over from the internal connection between its first input and its output to the internal connection between its second input and its output at a time instant mT prior to the time instant of the start of the supply of said block of information of the digital information signal, where m is an integer for which holds $m \geq 1$.
- 30 6. Apparatus as claimed in claim 5, characterized in that $m = n$.
7. Apparatus as claimed in anyone of the preceding claims, characterized in that $n=2$.
8. Encoding means for encoding a digital information signal so as to obtain a channel signal, the encoding means comprising a nT precoder, where n is an integer for



which holds $n \geq 1$, and T is the bittime in the digital information signal, the nT precoder comprising signal combination means and delay means for realizing a signal delay of nT , the encoding means further comprising switching means having a first and second input, an output and a control signal input, the second input of the switching means being coupled to
5 an output of the signal combination means, the output of the switching means being coupled to an input of the nT delay means.

9. Encoding means as claimed in claim 8, characterized in that $n=2$.

