(12) DEMANDE INTERNATIONALE PUBLIÉE EN VERTU DU TRAITÉ DE COOPÉRATION EN MATIÈRE DE BREVETS (PCT)

(19) Organisation Mondiale de la Propriété Intellectuelle
Bureau international

(43) Date de la publication internationale
16 janvier 2003 (16.01.2003)

PCT

(10) Numéro de publication internationale
WO 03/005434 A2

(51) Classification internationale des brevets[7] :
H01L 21/324, 21/306, 21/762, 21/302, 21/316

(21) Numéro de la demande internationale :
PCT/FR02/02341

(22) Date de dépôt international : 4 juillet 2002 (04.07.2002)

(25) Langue de dépôt : français

(26) Langue de publication : français

(30) Données relatives à la priorité :
0108859 4 juillet 2001 (04.07.2001) FR

(71) Déposant *(pour tous les États désignés sauf US)* : S.O.I.TEC SILICON ON INSULATOR TECHNOLOGIES [FR/FR]; Parc Technologique des Fontaines, Chemin des Franques, F-38190 Bernin (FR).

(72) Inventeurs; et

(75) Inventeurs/Déposants *(pour US seulement)* : NEYRET, Eric [FR/FR]; 2, rue Lesdiguières, F-38360 Sassenage (FR). ECARNOT, Ludovic [FR/FR]; 10 Lotissement le Nivolon, F-38760 Varces (FR).

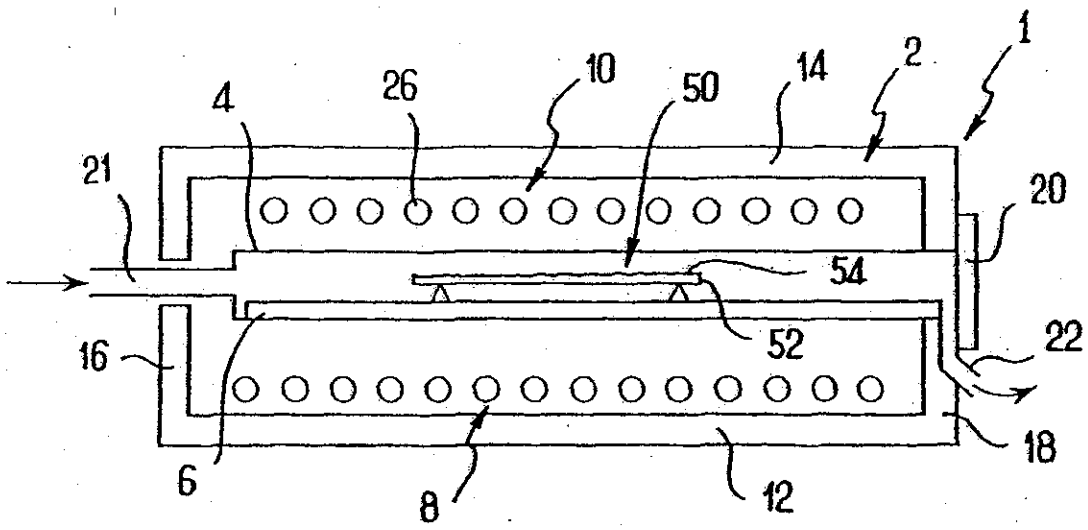
(74) Mandataires : MARTIN, Jean-Jacques etc.; Cabinet Regimbeau, 20, rue de Chazelles, F-75847 Paris Cedex 17 (FR).

(81) États désignés *(national)* : AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZM, ZW.

[Suite sur la page suivante]

(54) Title: METHOD FOR REDUCING SURFACE RUGOSITY

(54) Titre : PROCEDE DE DIMINUTION DE RUGOSITE DE SURFACE



(57) Abstract: The invention relates to a method for reducing the rugosity of the free surface of a slice of semiconductor material. Said method comprises an annealing step in order to smooth said free surface. The invention is characterized in that the method for reducing free surface rugosity comprising a single smoothing annealing step which is carried out in the form of rapid thermal annealing in an atmosphere which is exclusively comprised of pure argon. The invention also relates to a structure produced by said method.

(57) Abrégé : L'invention propose un procédé de diminution de la rugosité de la surface libre d'une tranche de matériau semiconducteur, ledit procédé comprenant une étape de recuit afin de lisser ladite surface libre, caractérisé en ce que le procédé de diminution de rugosité de surface libre comporte un unique recuit de lissage réalisé sous la forme d'un recuit thermique rapide sous une atmosphere composée exclusivement d'argon pur. L'invention propose également une structure réalisée par un tel procédé.

WO 03/005434 A2

WO 03/005434 A2

(84) États désignés *(régional)* : brevet ARIPO (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), brevet eurasien (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), brevet européen (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SK, TR), brevet OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Publiée :

— *sans rapport de recherche internationale, sera republiée dès réception de ce rapport*

En ce qui concerne les codes à deux lettres et autres abréviations, se référer aux "Notes explicatives relatives aux codes et abréviations" figurant au début de chaque numéro ordinaire de la Gazette du PCT.

METHOD FOR REDUCING SURFACE RUGOSITY

The present invention relates in general manner to the surface treatment of materials, and in particular to treating substrates for fabricating components for microelectronic and/or optoelectronic applications.

More precisely, the invention relates to a method of reducing the roughness of the free surface of a wafer of semiconductor material, said method including an annealing step in order to smooth said free surface.

The term "free surface" is used to mean the surface of a wafer which is exposed to the external environment (in contrast to an interface surface which is in contact with the surface of another wafer or some other element).

As explained below, the invention can be implemented in particularly advantageous, but non-limiting manner, in combination with a method of fabricating thin films or layers of semiconductor material of the type described in French patent No. 2 681 472.

A method reproducing the teaching of the above-cited document is known as the Smartcut® method. In outline, its main steps are as follows:

- a step of implanting atoms beneath a face of a substrate of semiconductor material (in particular silicon), in an implantation zone of the substrate;
- a step of putting the implanted substrate into intimate contact with a stiffener; and
- a step of cleaving the implanted substrate in its implantation zone so as to transfer the portion of the substrate that is situated between the surface that was subjected to implantation and the implantation zone to the stiffener, thereby forming a thin film or layer of semiconductor thereon.

The term "implanting" atoms covers any bombardment of atomic or ionic species suitable for introducing said species into the material of the wafer, with the implanted species having a concentration maximum at a

determined depth within the wafer relative to the bombarded surface, so as to define a zone of weakness.

The depth of the zone of weakness is a function of the nature of the implanted species, and the energy which is associated therewith for implantation.

In this text, the generic term "wafer" is used to designate the film or layer transferred by such a Smartcut® type method.

The wafer (which is made of semiconductor material) can thus be associated with a stiffener, and possibly also with other, intermediate layers.

The term "wafer" is also used in the present text, to cover any wafer, layer, or film of semiconductor material such as silicon, regardless of whether or not the wafer has been produced by a Smartcut® type method, the object in all cases being that of reducing the roughness of the free surface of the wafer.

For applications of the type mentioned at the beginning of this text, the roughness specifications associated with the free surfaces of wafers are very severe, and the quality of the free surfaces of wafers is a parameter which determines the quality of components to be made on the wafer.

It is thus common to find roughness specifications that must not exceed 5 angstroms (Å) in root mean square (rms) value.

Roughness measurements are generally performed using an atomic force microscope (AFM).

With that type of apparatus, roughness is measured on surfaces that are scanned by the tip of the AFM microscope, covering areas in the range 1 micrometer (µm) × 1 µm to 10 µm × 10 µm, and more rarely 50 µm × 50 µm, or even 100 µm × 100 µm.

Roughness may be characterized in two ways, in particular.

In one of these ways, the roughness constitutes so-called "high frequency" roughness and corresponds to scanning areas of about 1 µm × 1 µm.

In the other of these ways, the roughness is said to be "low frequency" roughness and corresponds to scanning areas of about 10 µm × 10 µm or greater. The 5 Å specification given above by way of indication is thus for roughness corresponding to a scan area of 10 µm × 10 µm.

Wafers produced by known methods (of the Smartcut® type or some other method) present surface roughnessses of values that are greater than specifications of the magnitude specified above, unless the surface of the wafer is subjected to specific treatment, such as polishing.

A first known type of method for reducing the surface roughness of wafers consists in subjecting the wafer to "conventional" heat treatment (e.g. sacrificial oxidation).

However, treatment of that type does not enable the roughness of wafers to be brought down to the level of the above-mentioned specifications.

Although, in order to further reduce roughness, it is possible to envisage increasing the number of applications of such conventional heat treatments, and/or combining them with other known types of method, that leads to a method that is lengthy and complex.

Thus, for example, European patent No. 1 061 565 discloses a method of that type, teaching lengthy annealing (about 60 minutes (min)) at high temperature, followed by cooling under an atmosphere containing hydrogen.

A second known type of method consists in subjecting the free surface of the wafer to chemical-mechanical polishing.

That type of method can indeed enable the roughness of the free surface of the wafer to be reduced.

When there exists a defect concentration gradient that increases towards the free surface of the wafer, that second known type of method can also serve to abraid said wafer down to a zone that presents an acceptable concentration of defects.

However, that second known type of method presents the drawback of compromising the uniformity of the free surface of the wafer.

That drawback is made worse when a large amount of polishing is performed on the surface of the wafer, as would be necessary in order to reach roughness levels of the kind mentioned above.

A third known type of method consists in subjecting the wafer to rapid annealing under a controlled atmosphere, known as rapid thermal annealing (RTA).

Below in this text, this form of annealing is referred to either by its acronym RTA or in full as "rapid thermal annealing".

In this third type of method, the wafer is annealed at high temperature, which may lie in the range about 1100°C to 1300°C, for a period of 1 second (s) to 60 s.

In a first variant of this third type of method, an example of which is to be found in US patent No. 6 171 965, the free surface of the wafer is smoothed by performing RTA of the wafer under an atmosphere constituted by a mixture generally comprising hydrogen in combination with reagent gases (HCl, HF, HBr, SF_6, CF_4, NF_3, CCl_2F_2, ...).

In this first variant of the third type of method, the aggressivity of the mixture constituting the annealing atmosphere enables the free surface of the wafer to be "etched", thereby reducing its roughness.

That first variant can present advantages.

However a limitation lies in the aggressive nature of the mixture of gases constituting the atmosphere used in such a method, and elements other than the free surface of the wafer may be exposed to the action thereof

(the face of the wafer or the structure to which it is bonded that faces away from said free surface of the wafer, and sometimes also the annealing chamber).

It can thus be necessary to take additional measures for protecting those elements, thereby tending to make the method even more complex.

The aggressivity of the mixture used can, under some circumstances, also worsen defects in the wafer, and that can likewise require additional treatments.

Furthermore, that variant using an annealing atmosphere made up of different gases, some of which are reactive, requires an installation to be provided for implementing such a method that can be relatively complex (feeds for different gases, safety measures, ...).

An implementation taught in European patent No. 1 061 565 corresponds to that first variant of the third type of method. In that implementation, RTA is performed in an atmosphere that always contains hydrogen.

In a second variant of that third type of method, the wafer is subjected to RTA under an atmosphere that does not have the function of attacking the material of the wafer.

In that variant, smoothing is the result not of etching the free surface of the wafer, but of rebuilding the surface of the wafer.

In that case, the annealing atmosphere is typically made up of hydrogen mixed with argon or nitrogen.

French patent application No. 99/10667 in the name of the Applicant discloses an example of that second variant of the third type of method.

European patent No. 1 158 581 discloses finishing treatment which always comprises two annealing operations, including one RTA operation, said annealing operations being performed in an atmosphere containing hydrogen or argon.

The two annealing operations taught by that document both serve to smooth the free surface of the wafer. The

reduction in low frequency roughness is illustrated by the last column of Table 2 in that document, which shows in particular the effect of the second annealing operation following the RTA operation.

With RTA treatment alone ("comparative example 1"), low frequency roughness after treatment is 1.60 nanometers (nm) rms. By implementing the two annealing operations taught by that document, the low frequency roughness is significantly improved, reaching values of 0.28 nm rms and 0.30 nm rms.

The teaching of EP 1 158 581 is thus focused on performing two successive operations of smoothing by annealing (where smoothing is characterized by a reduction in low frequency roughness), with the first of those two annealing operations being RTA.

However, the method taught by EP 1 158 581 is relatively lengthy and expensive to implement since it always requires two annealing operations for smoothing.

The invention seeks to provide an improvement to the methods mentioned above.

It would be advantageous to simplify such methods further.

In addition, it would also be advantageous to reduce any slip lines that can appear in the crystallographic structure of the material of the wafer, in particular as a result of heat treatment (such as that which might be applied to the wafer in order to cleave it when performing a Smartcut® type method).

It is known that such slip lines can result from heat being received non-uniformly in different regions of the wafer (where this is particularly troublesome in furnaces presenting cold spots).

Furthermore, the hydrogen used in prior implementations of this variant is a gas that is relatively expensive, whereas effort is continuously directed to reducing the costs associated with wafer treatment methods.

Finally, it would be particularly advantageous to be able to implement a method satisfying the above-mentioned objects in combination with a method of the Smartcut® type.

Disclosed herein is a method satisfying those needs.

In a first aspect, there is provided a method of reducing the roughness of the free surface of a wafer of semiconductor material, said method comprising a stage of annealing in order to smooth said free surface, the method being characterized in that the stage of reducing the free surface roughness comprises a single smoothing annealing operation implemented in the form of rapid thermal annealing under an atmosphere made up exclusively of pure argon.

Preferred but non-limiting embodiments of the method are as follows:

- the method also comprises the following prior steps:
  - ✓ a step of implanting atoms under a face of a substrate from which the wafer is to be made, in an implantation zone of the substrate;
  - ✓ a step of putting the implanted substrate into intimate contact with a stiffener; and
  - ✓ a step of cleaving the implanted substrate in the implantation zone in order to make the wafer out of the portion of the substrate that is situated between the surface subjected to implantation and the implantation zone, and transferring said wafer onto the stiffener;
- the rapid thermal annealing is performed with a high temperature dwell lying in the range 1100°C to 1250°C, for a period of 5 s to 30 s;
- the stage of rapid thermal annealing under pure argon is followed by a polishing stage;
- the polishing stage is followed by a sacrificial oxidation stage:

- the following stages are performed in succession:
  - ✓ sacrificial oxidation;
  - ✓ rapid thermal annealing under pure argon;
  - ✓ polishing; and
  - ✓ sacrificial oxidation;
- the stage of rapid thermal annealing under pure argon is followed by the following stages:
  - ✓ sacrificial oxidation;
  - ✓ polishing; and
  - ✓ sacrificial oxidation;
- the following succession of stages is performed:
  - ✓ rapid thermal annealing under pure argon;
  - ✓ polishing; and
  - ✓ rapid thermal annealing under pure argon;
- the stage of rapid thermal annealing under pure argon is preceded by a stage of sacrificial oxidation;
- the stage of rapid thermal annealing under pure argon is followed by a stage of sacrificial oxidation; and
- the stage of rapid thermal annealing under argon is preceded by a stage of sacrificial oxidation, and said stage of rapid thermal annealing under pure argon is followed by an additional stage of sacrificial oxidation.

In a second aspect, there is provided a silicon on insulator (SOI) structure obtained by such a method.

Other aspects, objects, and advantages of the invention appear better on reading the following description of preferred implementations of the invention, given with reference to the accompanying drawing, in which:

- Figure 1 is an overall and diagrammatic view in longitudinal section of an annealing chamber enabling the invention to be implemented; and
- Figure 2 is a graph showing the reduction in roughness obtained by implementing the invention on a silicon wafer.

With reference initially to diagrammatic Figure 1, there can be seen a non-limiting example of an annealing chamber 1 enabling the invention to be implemented.

The chamber is for implementing an annealing stage under a pure argon atmosphere using the RTA technique.

The chamber 1 comprises an enclosure 2, a reactor 4, a substrate-carrier tray 6, two arrays of halogen lamps 8, 10, and two pairs of side lamps.

The enclosure 2 comprises in particular a bottom wall 12, a top wall 14, and two side walls 16, 18 situated at respective longitudinal ends of the enclosure 2. One of the side walls 16, 18 includes a gate 20.

The reactor 4 is constituted by a quartz tube extending longitudinally between the two side walls 16, 18. At the respective side walls 16 and 18, it is provided with a gas inlet 21 and a gas outlet 22. The gas outlet 22 is situated in the side wall 18 that has the gate 20.

The arrays 8, 10 of halogen lamps are situated respectively above and below the reactor 4, between the reactor and the bottom and top walls 12 and 14.

Each array 8, 10 of halogen lamps comprises seventeen lamps 26 disposed perpendicular to the longitudinal axis of the reactor 4.

The two pairs of side lamps (not shown in Figure 1) are situated parallel to the longitudinal axis of the reactor 4, each on one side thereof, generally at the longitudinal ends of the lamps 26 in the arrays 8, 10 of halogen lamps.

The substrate-carrying tray 6 slides inside the reactor 4. It supports a wafer 50 that is to be subjected to a stage of annealing under a hydrogen-containing atmosphere 100 and enables wafers to be inserted and removed into and from the chamber 1. A chamber 1 of this type is sold by Steag® under the name "SHS AST 2800".

It is specified that the "wafer" 50 may be constituted in general manner by any single-layer or multi-layer structure having a surface layer of semiconductor material (such as silicon in preferred but non-limiting manner).

It is recalled that an object of the invention is to reduce the roughness of the free surface of such a surface layer.

The invention can be implemented to reduce the roughness of the free surface of a wafer 50 that has not been subjected to any prior treatment, and also to wafers that have been obtained by specific treatments.

In particular, different variants of the invention apply in particularly advantageous manner to reducing the roughness of the surface of an SOI structure and/or of a substrate of semiconductor material from which such a structure is obtained, in particular by applying a method of the Smartcut® type.

Thus, in the context of the Smartcut® method, the invention can advantageously be implemented for the purpose of reducing the roughness of one or the other of the two surfaces of semiconductor material obtained by cleaving the zone of weakness made during the implantation step, or for reducing the roughness of both of these surfaces.

The different variant implementations of the method of the invention described below by way of example are applied to treating wafers 50 having a useful layer of semiconductor material 52 (e.g. made of silicon), said layer itself having a free surface 54.

The layer 52 is said to be "useful" since it is to be used for making electronic, optical, or optoelectronic elements on the wafer 50.

As mentioned above, the free surface 54 may be a cleaved surface obtained by implementing a Smartcut® method.

When the wafer 50 is an SOI substrate obtained by the Smartcut® method, the wafer 50 comprises beneath the useful layer 52 a buried oxide layer itself covering a supporting substrate.

It should be understood that in Figure 1 the thickness of the wafer 50 has been exaggerated in order to show the useful layer 52 and its free surface 54.

The invention can thus be implemented solely by performing an RTA stage on the wafer 50 under an atmosphere of pure argon.

The stage of annealing under pure argon comprises the steps consisting in:

· placing the wafer 50 in the chamber 1, with the chamber being cold when the wafer is inserted;

· introducing an annealing atmosphere of pure argon into the chamber at a pressure equal to or close to atmospheric pressure. It should also be understood that this pressure could also be set at a lower value, lying in the range a few millitorr (mTorr) to atmospheric pressure;

· switching on the halogen lamps 26 so as to cause the temperature inside the chamber 1 to rise at a rate of about 50°C per second, up to a treatment temperature;

· maintaining the wafer 50 in the chamber 1 throughout the duration of a high-temperature dwell; and

· switching off the halogen lamps 26 and cooling the wafer 50 by means of a flow of air at a rate of several tens of degrees Celsius per second, with temperature varying in application of any desired relationship.

In this respect, it is particularly important for the argon that is used to be as pure as possible since the Applicant has found that the presence of small quantities of additional elements (such as oxygen in particular) can lead to the material of the useful layer being attacked (by forming highly volatile SiO if a surface area of silicon is exposed to an annealing

atmosphere that includes a small quantity of oxygen, for example).

The Applicant has found that such a stage of annealing under an atmosphere of pure argon enables the roughness of the free surface 50 to be decreased significantly.

The results obtained were in particular of much better quality than the reduction in roughness that can be obtained solely by conventional treatment such as heat treatment of the sacrificial oxidation type.

The uniformity of the useful layer is also much better than it would be if the wafer were to be subjected to a polishing operation.

The stage of RTA under pure argon may comprise, for example, a high temperature dwell having a duration of 5 s to 30 s, and a treatment temperature lying in the range 1100°C to 1250°C.

Figure 2 shows the reduction in roughness obtained by such a method. More precisely, this figure sets out the improvement in "haze" obtained by applying a method of the invention as described above.

In this figure, the abscissa axis relates to different wafers, with haze being measured for each wafer before applying annealing of the invention (top measurement) and after (bottom measurement).

In Figure 2, the top curve thus corresponds to haze as measured at the surface of SOI structures after they have been cleaved, and the bottom curve relates to the same measurements performed after RTA under argon at 1230°C with a high temperature dwell of 30 s.

The term "haze" designates the optical signal diffused by the surface of the substrate 50 in response to being excited by light. This haze is representative of surface roughness.

This characteristic which is representative of the surface roughness of the substrate was measured in the present case using equipment of the KLA Tencor® type, and

of the Surfscan 6220® model: the haze as measured is thus labeled by the reference "haze 6220".

It can be seen that the reduction in haze 6220 is of an amount that is comparable to the results that can be obtained by other RTA techniques, for example RTA under an atmosphere made of a mixture of hydrogen and argon.

More precisely, the improvement in haze corresponds to haze being divided by a factor of about 6 to 10.

Advantageously, implementing the method of the invention makes it possible to obtain results with this high level of quality while avoiding the limitations mentioned above relating to prior RTA techniques.

In particular, since argon is an excellent conductor of heat, using an atmosphere of pure argon enables heat to be spread in a manner that is as uniform as possible inside the chamber 1, thereby reducing the slip lines that can be observed when implementing those prior methods.

As mentioned above, the invention can be implemented solely by the stage of RTA under pure argon: this stage makes it possible to obtain a considerable improvement in the surface state of the wafer 50.

In addition, this improvement is obtained with practically no material being removed from the wafer, but on the contrary with the surface 54 being rebuilt and smoothed.

Several variant implementations of the invention are described below involving not only the stage of RTA under pure argon, but also additional treatment stages.

In a first variant, the stage of RTA under pure argon is followed by a stage of polishing the surface of the wafer 50.

This polishing stage is implemented by conventional chemical-mechanical polishing.

It serves to remove material from the working layer 52 situated close to the free surface 54 and which might still contain surface defects.

In a second variant, the stage of RTA under pure argon is followed not only by a polishing stage, but also by a subsequent additional stage of sacrificial oxidation combined with heat treatment.

The sacrificial oxidation stage is intended to reduce any defects that might remain after the following stage. When implementing the invention after a Smartcut® method, defects may be associated with the implanting stage or the cleaving stage.

The sacrificial oxidation stage comprises an oxidation step and a de-oxidation step.

The heat treatment is interposed between the oxidation step and the de-oxidation step.

The oxidation step is preferably performed at a temperature lying in the range 700°C to 1100°C.

The oxidation step may be performed by a dry technique or by a wet technique.

In the dry technique, the oxidation step is performed, for example, by heating the wafer 50 under gaseous oxygen.

In the wet technique, the oxidation step is performed, for example, by heating the wafer 50 in an atmosphere charged with steam.

In both the dry technique and the wet technique, in conventional methods known to the person skilled in the art, the oxidizing atmosphere may also be charged with hydrochloric acid.

The oxidation step leads to an oxide 60 being formed covering the surface 54 of the useful layer 52.

The heat treatment stage is performed by any heat treatment operation serving to improve the qualities of the material constituting the useful layer 52.

The heat treatment may be performed at constant temperature or at varying temperature.

With varying temperature, heat treatment is performed, for example, by progressively raising

temperature between two values, or with temperature oscillating cyclically between two values, etc.

The heat treatment stage is preferably performed at least in part at a temperature higher than 1000°C, and more particularly around 1100°C to 1200°C.

This heat treatment is preferably performed under a non-oxidizing atmosphere, which may comprise argon, nitrogen, hydrogen, etc., or indeed a mixture of these gases. The heat treatment may also be performed in a vacuum.

Also preferably, the oxidation step is performed prior to the heat treatment stage.

In this way, the oxide 60 protects the remainder of the useful layer during the heat treatment and avoids the phenomenon of pitting.

Pitting is a phenomenon that is well known to the person skilled in the art and occurs at the surface of certain semiconductors when they are annealed under a non-oxidizing atmosphere such as nitrogen, argon, in a vacuum, etc. It occurs in particular with silicon when it is bare, i.e. when it is not covered at all in oxide.

In an advantageous variant, the oxidation step begins at the beginning of the rise in temperature of the heat treatment and it terminates before the end of the heat treatment.

The heat treatment serves to cure at least in part the defects generated during the preceding stages in the method of fabricating and treating the wafer 50.

More particularly, the heat treatment may be performed for a duration and at a temperature such as to enable it to cure crystal defects, such as stacking defects, "HF" defects, etc. generated in the useful layer 52 during the oxidation step.

The term "HF" defect is used to designate any defect whose presence is revealed by a decorative halo in the buried oxide which is situated under the useful layer 52 (when the wafer 50 is an SOI wafer obtained by a

Smartcut® method), after the wafer has been treated in a bath of hydrofluoric acid.

The heat treatment also presents the advantage of reinforcing the bonding interface, e.g. between the layer transferred during the transfer of the Smartcut® method and the supporting substrate.

The de-oxidation step is preferably performed in solution.

By way of example, the solution is a hydrofluoric acid solution at 10% or 20%. A few minutes suffice to remove one thousand to a few thousand angstroms of oxide 60, when the wafer 50 is dipped in such a solution.

In a third variant, the stages of the second variant described above are preceded by an additional stage of sacrificial oxidation of the surface of the wafer 50, this sacrificial oxidation (identical to that described above) preferably being combined with heat treatment.

The stages of RTA under pure argon and of chemical-mechanical polishing in this variant are identical to those described for the other variants described above.

As for the above-described sacrificial oxidation stage, the first and second sacrificial oxidation stages both comprise an oxidation step and a de-oxidation step.

The first and second sacrificial oxidation stages and the heat treatment steps are analogous to hose described for the second above-described variant of the method in accordance with the present invention.

In a fourth variant of the invention, the stage of RTA under pure argon is followed by two stages of sacrificial oxidation of the free surface of the wafer 50.

These sacrificial oxidation stages are identical to those described above and are preferably combined with heat treatment as described above.

In this variant, an additional chemical-mechanical polishing stage is interposed between the two sacrificial oxidation stages.

In a fifth variant of the invention, two stages of RTA under pure argon are performed on the wafer 50, with these two stages having interposed between them a chemical-mechanical polishing stage.

In a sixth variant of the invention, a sacrificial oxidation stage is performed on the surface of the wafer 50 (which stage is still identical to those described above, and is preferably combined with heat treatment), after which the wafer 50 is subjected to RTA under an atmosphere of pure argon.

In a seventh variant of the invention, the order of the two main stages of the sixth variant is reversed, with RTA under pure argon being performed before sacrificial oxidation.

In an eighth variant of the invention, between two stages of sacrificial oxidation of the surface of the wafer 50 (which stages are still identical with those described above, and preferably combined with heat treatment), there is interposed a stage of RTA of the wafer under pure argon.

It should be observed that the different variants of the invention as described above all make use of a single annealing operation for smoothing purposes.

This single smoothing annealing operation corresponds to rapid thermal annealing under an atmosphere made up solely of pure argon.

Some of the variants may also make use of other types of annealing, with those annealing operations not serving to smooth the free surface of the wafer.

In particular, the heat treatments associated with the sacrificial oxidation operations serve to withdraw material and to reinforce the bonding interfaces, and not to smooth the free surface of the wafer.

Although the sacrificial oxidation operations may have an effect on the roughness of the free surface of the wafer, it should be understood that this effect is not in any way comparable with the effect that is

expected during "smoothing" which seeks, as mentioned above, to reduce the low frequency roughness of the free surface of the wafer in significant manner.

Thus, typically, low frequency roughness of the free surface of a wafer can be reduced by a factor of 1 to 2 by a sacrificial oxidation technique, whereas the reduction is of the order of a factor of 10 when performing RTA (in this respect reference can be made to the table on page 19 of French patent No. 2 797 713).

It is also stated in particular that the teaching relating to the heat treatments associated with sacrificial oxidation satisfy a need that is quite different from the aim of smoothing.

In particular, the teaching of French patent No. 2 777 115 relating to such heat treatments included in a sacrificial oxidation operation and mentioning the possibility of using an atmosphere of argon cannot be transposed to the circumstances of the present invention in which an essential element lies in heat treatment in RTA mode.

A characteristic which is essential and common to all of the variants described above is thus that of the method of reducing free surface roughness having only a single smoothing annealing operation that is implemented in the form of rapid thermal annealing under an atmosphere made up exclusively of pure argon.

CLAIMS

1. A method of reducing the roughness of the free surface of a wafer of semiconductor material, said method comprising a stage of annealing in order to smooth said free surface, the method being characterized in that the stage of reducing the free surface roughness comprises a single smoothing annealing operation implemented in the form of rapid thermal annealing under an atmosphere made up exclusively of pure argon.

2. A method according to the preceding claim, characterized in that it also comprises the following prior steps:

- a step of implanting atoms under a face of a substrate from which the wafer is to be made, in an implantation zone of the substrate;
- a step of putting the implanted substrate into intimate contact with a stiffener; and
- a step of cleaving the implanted substrate in the implantation zone in order to make the wafer out of the portion of the substrate that is situated between the surface subjected to implantation and the implantation zone, and transferring said wafer onto the stiffener.

3. A method according to either preceding claim, characterized in that the rapid thermal annealing is performed with a high temperature dwell lying in the range 1100°C to 1250°C, for a period of 5 s to 30 s.

4. A method according to preceding claim, characterized in that the stage of rapid thermal annealing under pure argon is followed by a polishing stage.

5. A method according to the preceding claim, characterized in that the polishing stage is followed by a sacrificial oxidation stage.

6. A method according to any one of claims 1 to 3, characterized in that the following stages are performed in succession:

- sacrificial oxidation;
- rapid thermal annealing under pure argon;
- polishing; and
- sacrificial oxidation.

7. A method according to any one of claims 1 to 3, characterized in that the stage of rapid thermal annealing under pure argon is followed by the following stages:

- sacrificial oxidation;
- polishing; and
- sacrificial oxidation.

8. A method according to any one of claims 1 to 3, characterized in that the following succession of stages is performed:

- rapid thermal annealing under pure argon;
- polishing; and
- rapid thermal annealing under pure argon.

9. A method according to any one of claims 1 to 3, characterized in that the stage of rapid thermal annealing under pure argon is preceded by a stage of sacrificial oxidation.

10. A method according to any one of claims 1 to 3, characterized in that the stage of rapid thermal annealing under pure argon is followed by a stage of sacrificial oxidation.

11. A method according to any to any one of claims 1 to 3, characterized in that the stage of rapid thermal annealing under argon is preceded by a stage of sacrificial oxidation, and said stage of rapid thermal

annealing under pure argon is followed by an additional stage of sacrificial oxidation.

12. An SOI structure obtained by a method according to any preceding claim.