ABSTRACT

CHIP SCALE PACKAGE WITH OPEN SUBSTRATE

A method for manufacturing an integrated circuit package comprises forming a substrate by forming a core layer with a through opening and vias. A first conductive layer is formed on the core layer covering the through opening and a second conductive layer is formed on the core layer opposite the first conductive layer in the through opening and in the vias contacting the first conductive layer. An integrated circuit die is bonded to the second conductive layer and in the through opening. Connections are formed between the integrated circuit die and the second conductive layer, and the integrated circuit die and the connections are encapsulated. (Fig. 1)