SOI SUBSTRATES WITH A FINE BURIED INSULATING LAYER

TECHNICAL FIELD OF THE INVENTION

The present invention relates to a method of producing substrates by means of the direct wafer bonding of two substrates made from materials chosen from among semiconductor materials, the final structure thereby obtained being intended, in particular, for applications in the fields of electronics, optics, photovoltaics or optoelectronics.

To be more precise, this final structure is a Semiconductor On Insulator (SeOI), more particularly an SOI (Silicon On Insulator) substrate, characterised by an extremely thin (under 50 nm), buried insulator. In the event that the thin insulator should be an oxide, the substrate is said to be of an UTBOX (ultra-thin buried oxide) type. This final structure is achieved by direct wafer bonding a so-called "donor" substrate to a so-called "receiver" substrate, then thinning down the donor substrate with a view to transferring a generally thin layer of material from said donor substrate to the receiver substrate.

STATE OF THE ART

Direct wafer bonding is a technique that enables two substrates with perfectly flat surfaces to be directly adhered to one another without the use of adhesives (paste, glue, etc.). This type of bonding is a technological step commonly used in the production of SOI and SeOI structures.

There are three basic methods of producing SeOI or SOI structures by direct bonding: SMART CUT™, BSOI (and BESOI), and ELTRAN®. A description of the procedures involved in each of these methods can be found in the publication "Silicon wafer bonding technology for VLSI and MEMS applications", S.S. Lyer and A.J. Auberton-Hervé, IEE (2002).

The SOI substrates obtained by direct wafer bonding according to these different methods include a buried insulating layer. Consequently, in order to create an insulating layer of silicon oxide (SiO_2) on the original silicon substrate or substrates, thermal treatment can be applied in order to achieve wet or dry thermal oxidation of the silicon in the substrate surface. Alternatively, common depositing techniques such as CVD (Chemical Vapour Deposition), LPCVD (Low Pressure Chemical Vapour Deposition) and PCVD (Plasma Chemical Vapour Deposition) can also be used.

The thickness of the thermal or deposited oxide layers varies depending on the final structure required, in other words, depending on the thickness of the buried insulating layer sought. In order to produce UTBOX substrates, the buried insulating layer has a thickness under 50 nm, preferably between 5 nm and 25 nm.

However, the thinness of the insulating layer of the UTBOX substrates makes molecular bonding difficult and indirectly affects the quality of the final substrate. Based on a constant production method, an SOI substrate characterised by a so-called thick buried Insulator (typically with a thickness of over 100 nm) statistically exhibits far fewer bonding defects, as revealed following low-level thermal treatment, than a substrate with a very thin buried insulator.

In fact, with UTBOX structures, the species present at bonding interface level, such as water, hydrogen, hydrocarbons or species resulting from an implantation stage, can no longer find sufficient trapping sites within the thin oxide layer and diffuse along the bonding interface where they coalesce, giving rise to numerous structural defects.

In the case of a thin layer transfer using Smart Cut™ technology, the main defects exacerbated on the final structures by the extreme thinness of the buried insulator are referred to as "blisters" and "non-transferred zones". As is shown in Figure 1, they lead to holes of different sizes in the active layer 10, but these are always "killer" defects for the device produced from these substrates.

The non-transferred zones 200, known by the abbreviation "NTZ" or else referred to as "voids", are holes in the active layer 10 and the buried insulator 3 of a size typically between 0.1 µm and 3 mm. An NTZ 200 corresponds to a zone in an active layer 10 resulting from a donor substrate 1, also referred to as the first substrate, which is not transferred to the receiver substrate 2, also referred to as the second substrate. When these NTZ's are localised on the periphery of the final structure, more precisely at a distance typically between 1 and 5 mm from the edge of the substrate, they are referred to as edge voids 300.

An edge void 300 is a hole with a diameter typically between 50 µm and 3 mm in the thin transferred layer 10.

A blister 400 corresponds to a zone of transferred film that is removed from the receiver substrate 2 under pressure from an accumulated gas bubble at the bonding interface. Since the film that is lifted locally is very fragile, a blister 400 invariably leads to a hole in the final structure, with a diameter typically between 0.5 and 3 mm.

All holes in the centre or on the edge of the wafer, whether microscopic or macroscopic in size, are killer defects, because in the absence of an active layer for the creation of electronic components, no component can be produced on this site. NTZ's 200, edge voids 300 and blisters 400 are therefore synonymous with a decline in quality and a drop in yield.

In order to reduce the number of defects associated with the bonding stage and reinforce the bonding interface, the substrates may undergo plasma activation before they are brought into contact. "Plasma

activation" of a bonding surface is defined as the exposure of this surface to plasma (which, notably, may take place in a vacuum or at atmospheric pressure).

More precisely, in the known activation techniques, the surface of a section to be activated is exposed to plasma at an exposure stage in which the exposure parameters are controlled, so that each one is set at a given value that remains fixed throughout the plasma activation.

The principle "exposure parameters" are:

- power density. This is the power density supplied to the plasma, which translates a power density by unit area (W/cm^2) and will likewise be referred to in this text simply using the term "power".
- pressure (pressure in the vessel holding the plasma),
- the nature and output of the gas supplying this vessel,
- the activation duration.

Activation of this type makes it possible, in particular, to execute direct wafer bonding by achieving significant bonding energies without having to resort to thermal treatment which must, necessarily, be carried out at high temperatures.

In effect, plasma activation makes it possible to obtain high bonding energies between two substrates, at least one of which has been activated prior to bonding, following thermal treatment carried out for relatively short durations (around 2 hours, for example) and at relatively low temperatures (around 600 °C or less, for example).

Activation of this type is therefore advantageous in stabilising a structure comprising two bonded substrates, if the intention is to avoid subjecting the structure to excessively high temperatures (particularly in the case of heterostructures, which are defined as structures made up of layers of materials with significantly different thermal expansion coefficients).

Activation of this type may also be advantageous in achieving significant bonding strengths at a given temperature.

Activation of this type is therefore advantageous, for example, in achieving multilayer structures involving the bonding of two substrates.

The transfer procedures (particularly Smart Cut™ procedures for which a general description is given in the publication SILICON-ON-INSULATOR TECHNOLOGY: Materials to VLSI, 2nd Edition (Jean-Pierre COLINGE), or BESOI (Bond Etch Silicon On Insulator) procedures, in which two substrates are bonded then the surplus material is removed from one of the substrates by etching, or ELTRAN™) procedures are examples of applications that can benefit from plasma activation to support bonding.

In order to benefit fully from the effects of plasma treatment for each bonding, the standard procedure found in the literature (notably in the documents entitled *Effects of plasma activation on hydrophilic bonding of Si and SiO_2,* T. Suni and I. J. Electroch. Soc. Vol. 149, n°6, p.348 (2002) and in the American patent US 6 180496 by Farrens et al.) involves the plasma activation of one or both bonding substrates.

Different gases are used today in plasma treatments, in order to activate the wafer surfaces before they are brought into contact, including, for instance, oxygen, nitrogen and argon.

However, although the various techniques currently used favour a high bonding energy at the interfaces, they do not allow very high quality semiconductor structures to be produced with thin or even ultra-thin insulating layers.

SUMMARY OF THE INVENTION

The aim of the invention is to produce an SeOI semiconductor structure with a high-quality thin buried insulating layer, presenting a thickness between 2 and 25nm, and the lowest possible defectivity, thanks in particular to a reinforced bonding interface.

Another aim of the invention is to develop a simplified and less onerous method of producing SeOI structures with a thin buried insulating layer. The insulator for burying is traditionally obtained by thermal oxidation or deposition, a stage that is itself preceded by wet cleaning. The invention enables these stages to be eliminated by forming the insulator with the aid of plasma treatment, which simplifies the procedure, removes the costs associated with cleaning and forming the insulator and reduces the thermal budget.

The elimination of a cleaning stage makes it possible to avoid any increased roughness associated with this stage and therefore to improve the quality of the subsequent bonding.

The sharp reduction in the thermal budget associated with the elimination of the insulator depositing or thermal treatment stage (e.g. thermal oxidation of the silicon) forming the insulator makes it possible to limit the number of defects produced at temperatures higher than 600 °C, such as dislocations or other defects associated with thermal treatment, such as slip lines or also oxide precipitates that can appear within the substrates treated.

In accordance with the invention, this aim is achieved by:

forming at least one insulating layer 3, 4 on a surface 3' of a first substrate and/or on a surface 4' of a second substrate 2, said surfaces 3', 4' being free from an insulator or presenting a native oxide layer resulting from exposure of the substrates to the ambient; assembling said first and second substrates 1 and 2; thinning down said first substrate 1, the insulating layer forming stage consists in a plasma activation based on oxidising and/or nitriding gas.

To be more precise, an advantageous application of the invention involves the production of SeOI substrates characterised by a thin buried insulator, more especially UTBOX (Ultra-Thin Buried Oxide) SOI substrates with a thickness of under 25 nanometres, around ten or so nanometres, for example.

This method of producing SeOI structures may be used with a view to transferring a thin layer by direct wafer bonding with a thinning-off of the substrate (using a Smart Cut™ transfer or other method, for example).

BRIEF DESCRIPTION OF THE FIGURES

Other features and advantages of the invention will emerge from the description of it given below, with reference to the attached drawings that represent several possible embodiments, these being given by way of example without being in any way restrictive.

In these drawings:

- Figure 1 is a diagram representing different defects that may be present in an SeOI substrate.
- Figures 2A to 2E are diagrams representing successive stages in a first embodiment of the inventive procedure.
- Figures 3A to 3F and 4A to 4F are diagrams representing successive stages of a second and third embodiment of the inventive procedure.
- Figure 5 is a sectional view by transmission electron microscopy of an UTBOX SOI substrate with a buried insulating layer 10 nm thick, achieved by the second embodiment of the inventive procedure.

Identical, similar or equivalent sections of the various figures described below have the same numerical references, making it possible to move from one figure to the next.

DESCRIPTION OF THE INDIVIDUAL EMBODIMENTS

There now follows a brief description of the different successive stages in a first embodiment.

Figure 2A represents a first semiconductor substrate 1 with a front face 3', while Figure 2B represents a second substrate 2 with a front face numbered 4'. Each of the front faces of the substrates 1 and 2 undergoes plasma treatment in accordance with Figures 2C and 2D. An insulating layer is deliberately not created on the surface of substrates 1 and 2 before they undergo the plasma treatment according to the invention. Furthermore, a native oxide layer resulting from exposure of the substrates to the ambient air may be present on the surface of these substrates.

Hence, the front face 3' of the first substrate 1 is subjected to treatment based on oxidising gas, such as oxygen, water or nitrogen protoxide, in order to create an insulating layer 3 on the surface of substrate 1. If the plasma oxidising treatment is carried out with oxygen, the pressure range is around 5 to 200 mT, the power range around 10 to 4000 W, the output around 10 to 1000 sccm, and this lasts for between 1 sec and 300 secs, in order to create the insulating layer 3 with a thickness varying between 2 nm and 15 nm.

By way of example, the first substrate 1 is subjected to oxygen plasma at a pressure of 15 mT, a power of 1000 W and an output of 100 sccm for a duration of 30 secs, in order to produce an SiO_2 insulating layer 3 with a thickness of 8 nm.

Optionally, the front face 4' of the second substrate 2 may be subjected to plasma nitriding treatment; the nitriding gas may be chosen from among nitrogen, nitrogen dioxide, ammonium, nitrogen monoxide and nitric acid, with the general plasma nitriding conditions falling within a pressure range of 5 to 200 mT, a power range of 10 to 4000 W and an output range of 10 to 1000 sccm for a duration of between 1 and 300 secs,

in order to create an insulating layer 4 with a thickness of between 2 nm and 15 nm.

However, since this second plasma treatment is optional, the second substrate 2 may be brought into direct contact with the first substrate 1.

In the present case, the front face 4' of the second substrate 2 is subjected to nitrogen plasma at a pressure of 50 mT, a power of 1000 W and an output of 200 sccm for a duration of 45 secs, in order to produce a nitrided layer with a thickness of 5 nm.

Whichever of the two substrates 1 or 2 it is executed on, the plasma treatment performed not only enables a fine insulating layer to be created, but also the substrate surfaces treated to be activated, in order to achieve good quality bonding with an energy of some 500 mJ/cm^2 or more.

It is important to underline that whatever the plasma oxidising or nitriding applied, the proportion of gas or gases used may be constant or variable during the treatment. Hence, it is possible to envisage that the proportion of oxidising gas falls as the proportion of nitriding gas rises and, conversely, that the proportion of nitriding gas falls as the proportion of oxidising gas rises.

In general terms, the plasma treatment parameters are adjusted, in order to control the thickness of the insulating layer 3, 4 formed by plasma on one and/or the other of the substrates and therefore the total thickness of the insulator buried in the final structure.

In all cases, plasma treatment leads to the formation of a single or multiple insulating layer, which may be made from silicon oxide (SiO_2), silicon nitride (Si_3N_4) or silicon oxynitride ($Si_xO_yN_z$) or may be of any other nature, depending on the plasmas used.

Thanks to this technique, a fine insulating layer is formed in the substrate surfaces, without any material whatsoever being provided, contrary to the depositing techniques that can likewise be used. In fact, the plasma treatment described in the present invention consists of a

modification and/or consumption of the substrate surface treated, in order to oxidise, nitride or even oxynitride the surface of this substrate.

Preparation of the front faces 3' and 4' of the substrates prior to plasma treatment can be envisaged, such as, for example, cleaning, brushing or drying treatments. Hence, standard cleaning treatments can be applied to at least one of the two surfaces, such as, for example, RCA treatment that involves subjecting the substrates to a first solution made up of a mixture of ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2) and deionised water, followed by a second solution comprising a mixture of hydrochloric acid (HCl), hydrogen peroxide (H_2O_2) and deionised water.

The front faces 3' and 4' of the substrates 1 and 2 may be non-oxidised, non-nitrided, in other words, in general terms free from an insulator (oxyde or nitride or oxynitride), or they may bring to their surface a native layer resulting from exposure of the substrates to the ambient air, such as, for example, native oxygen of around a few nm, more particularly with a thickness of under 3 nm.

The two substrates 1 and 2 with their respective insulating layers 3 and 4 are then brought into close contact for assembly by molecular bonding to achieve the SeOI structure 6, as is shown in Figure 2E. The structure 6 is made up successively of the substrate 2, the insulating layers 4 and 3 and the substrate 1.

According to the example described above, the first insulating layer 3 in SiO_2 measuring 8 nm is brought into contact with the second nitrided insulating layer 4, which is 5 nm thick, so that the final structure 6 has an insulating layer with a final thickness of 13 nm.

Two other embodiments are now going to be described in relation to Figures 3A to 3F and 4A to 4F.

The same elements have the same numerical references and will not be described again.

Figures 3A and 3F illustrate an embodiment of the invention that uses the SMART CUT™ procedure. For a more detailed

description of this type of implantation procedure, please consult the publication "Silicon on insulator technology: materials to VLSI", 2nd edition, Jean-Pierre COLINGE.

Figure 3A shows a first substrate 1 with its front face 3', whereas Figure 3B shows the same first substrate 1 undergoing an atomic and/or ionic species implantation stage.

The purpose of this implantation is to create a weakened zone 5 within the first substrate 1, which defines a thin, so-called active layer 10 in a section referred to as 100 of the first substrate 1.

It is likewise possible to carry out a co-implantation of atomic and/or ionic species with, for example, the implantation of hydrogen and helium species.

As illustrated in Figure 3C, the first substrate 1 is subjected to plasma nitriding treatment. For example, ammonium plasma is achieved at a pressure 50 mT, a power of 500 W and an output of 200 sccm for a duration of 45 secs, in order to create a nitrided insulating layer 3 with a thickness of 4 nm.

In relation to the second substrate 2, it undergoes plasma oxidising treatment according to the methods described later. Hence, for example, oxygen plasma is applied at a pressure of 50 mT, a power of 500 W and an output of 200 sccm for a duration of 45 secs, In order to create an insulating layer 4 in SiO_2 with a thickness of 6 nm.

In general terms, plasma treatments are carried out at low temperatures, in other words, at a temperature below 200 °C, more precisely, under 100 °C, or even at ambient temperature. Preferably, the plasma treatment is performed on an RIE type of plasma equipment (i.e. Reactive Ion Etching) at a temperature below 50°C.

Optionally, a thermal treatment may be applied to the insulating layers 3, 4 formed in the surface of the substrates 1 and/or 2 prior to bonding following the treatment according to the invention. This thermal treatment involves subjecting the substrates to a temperature of between 50 °C and 350 °C for between 30 mins and 5 hrs, in order to improve the

electrical and/or physical properties of the insulating layer 3, 4 formed on one or the other of the substrates 1, 2.

This is then followed by the direct wafer bonding of the second substrate 2 and the first substrate 1, bringing the insulating layer 3 of the first substrate 1 into close contact with the insulating layer 4 of the second substrate 2. This stage is shown in Figure 3E.

Prior to the plasma treatment stages of substrates 1 and 2 shown in Figure 3C and 3D, it is possible, as an option, to carry out a cleaning stage of the substrate surfaces to be treated, as described previously.

Finally, as shown in Figure 3F, the first substrate 1 is thinned down by detaching a section 100 of said first substrate 1, so as to obtain a composite SeOI structure, referred to as 6', made up successively of the second substrate 2, the stack of insulating layers 4 and 3 and a thin active layer 10.

The section 100 is detached along the weakened zone 5, through the application of mechanical, chemical and/or thermal forces, such as by thermal treatment between 200 °C and 500 °C, for example.

The final structure 6' thereby comprises an alternation of oxide and nitride layers not limited to this exact stacking. In fact, it is possible to envisage all possible alternations depending on the nature and number of the insulating layers present. For different applications, it is in fact possible to apply at least two plasma treatments in succession on one or both substrates.

In general terms, the final insulating layer of the structure 6' formed by stacking the insulating layers obtained by the different plasma treatments has a thickness of between 2 and 25 nm.

According to the example described previously, the first nitrided insulating layer 3 measuring 4 nm is brought into contact with the second insulating layer 4 of SiO_2, which is 6 nm thick, so that the final structure 6 has an insulating layer with a final thickness of 10 nm. Figure 5 shows a sectional view by transmission electron microscopy of this sort of

final structure, in this case an UTBOX SOI substrate with a buried insulator 10 nm thick, obtained from the second embodiment according to the invention.

Optionally, the structure 6' undergoes a finishing treatment involving at least one thinning and/or smoothing stage chosen from among dry or wet etching, oxidation/deoxidation, polishing and thermal treatment (such as Rapid Thermal Anneal (RTA) or long annealing in a neutral or reducing atmosphere).

In the third embodiment shown in Figures 4A to 4F, the weakened zone 5' is made up of a porous layer obtained, for example, by a procedure known to the person skilled in the art as ELTRAN™.

Hence, Figure 3B shows the first substrate 1 including this porous layer 5' defining a thin, so-called active layer 10 of a section 100 of the first substrate 1. As shown in Figure 3C, the first substrate 1 is subjected to plasma treatment in an oxidising atmosphere, in order to create an insulating layer 3 on the front face 3' of the first substrate 1.

Prior to the plasma treatment stage of the first substrate 1 and before the latter is assembled with the second substrate 2, as shown in Figure 4E, it is possible for an optional cleaning stage of surfaces 3' and 4' to be carried out.

Bonding of the first substrate 1 and of the second substrate 2 is carried out by bringing the insulating layer 3 into close contact with the front face 4' of the substrate 2.

Thermal treatment may be applied in order to reinforce the bonding interface. A thermal budget of between 200 °C and 1100 °C is thereby applied for between 30 mins and 20 hours.

Elimination of the section 100 of the first substrate 1 is carried out by applying mechanical forces, by mechanical-chemical polishing, by providing thermal energy and/or by chemical attack, through the application of a liquid, such as a pressurised water jet at the level of the weakened zone 5', or else by grinding or etching, as shown in Figure 4F.

The final structure obtained as a result of this third embodiment is referred to as 6" and differs from the aforementioned substrate 6' in that the bonding interface includes a single insulating layer: insulating layer 3.

Finally, although this is not shown in the figures, it will be noted that other embodiments of the inventive procedure may be used, notably by applying not a single oxidising and/or nitriding plasma to the first substrate 1, but a single plasma oxidising and/or nitriding treatment to the second substrate 2 prior to bonding with the first substrate 1, or else by combining different plasma treatments on one or both substrates to be assembled. It can therefore be envisaged that at least two plasma treatments are applied in succession to one or both substrates.

The substrates 1 and 2 are semiconductor materials and can be chosen from between crystalline-oriented silicon (100), or (110), or (111), polycrystalline silicon, silicon carbide, germanium and gallium arsenide. The second substrate 2 may likewise be made from sapphire, quartz, translucent fused quartz or also glass.

Thanks to these plasma treatments applied to the first substrate 1 and/or the second substrate 2, an insulating layer and an activated surface are formed in a single stage, resulting in a good quality bond, while anticipating the quality of the substrates treated and limiting the thermal budgets applied.

The sharp reduction in the thermal budget associated with the suppression of the insulator deposition or thermal treatment stage (e.g. thermal oxidation of the silicon) forming the insulator makes it possible to limit the number of defects generated at temperatures of over 600 °C, so that dislocation slip lines or else oxide precipitates may appear within the substrates treated.

This also makes it possible for substrates to be recycled. In fact, it is possible to reuse section 100 of the first substrate 1 for at least a second active layer 10 transfer onto a new second substrate 2.

CLAIMS

1. A method of producing a semiconductor structure 6, 6', 6''' with a fine buried insulating layer presenting a thickness between 2 and 25nm, including the following stages:
    - Forming at least one insulating layer 3, 4 on a surface 3' of a first substrate 1 and/or on a surface 4' of a second substrate 2, said surfaces 3', 4' being free from an insulator or presenting a native oxide layer resulting from exposure of the substrates to the ambient
    - assembling said first and second substrates 1 and 2,
    - thinning down said first substrate 1, in order to obtain said semiconductor structure,

    characterised in that the insulating layer forming stage consists in a plasma activation based on an oxidising and/or a nitriding gas.

2. The method according to claims 1, characterised in that the oxidising gas is chosen from among nitrogen, nitrogen dioxide, nitrogen monoxide, ammonium, nitric acid.

3. The method according to any of the claims 1 and 2, characterised in that the nitriding gas is chosen from among nitrogen, nitrogen dioxide, nitrogen monoxide, ammonium, nitric acid.

4. The method according to any of the claims 1 to 3, characterised in that the first substrate 1 and the second substrate 2 are made of silicon and in that the insulating layer 3, 4 is a silicon oxide (SiO_2), silicon nitride (Si_3N_4) or silicon oxynitride ($Si_xO_yN_z$) layer.

5. The method according to any of the claims 1 to 4, characterised in that the insulating layer 3, 4 of the semiconductor structure 6, 6', 6'' corresponds to an alternation of oxide and nitride layers.

6. The method according to any of the claims 1 to 5, characterised in that the power of the oxidising and/or nitriding gas is between 10 W and 4000 W.

7. The method according to any of the claims 1 to 6, characterised in that the oxidising and/or nitriding gas pressure is between 5 mT and 200 mT.

8. The method according to any of the claims 1 to 7, characterised in that the oxidising and/or nitriding gas output is between 10 sccm and 1000 sccm.

9. The method according to any of the claims 1 to 8, characterised in that the plasma exposure time is between 1 second and 300 seconds.

10. The method according to any of the claims 1 to 9 characterised in that at least two plasma activations are applied in succession to one or both substrates.

11. The method according to any of the claims 1 to 10, characterised in that the plasma activation is applied at temperatures below 200 °C.

12. The method according to any of the claims 1 to 11, characterised in that the plasma activation is applied at ambient temperature.

13. The method according to any of the claims 1 to 12, characterised in that the first substrate 1 and/or the second substrate 2 are chosen from between crystalline-oriented silicon (1,0,0), (1,1,0), or (1,1,1).

14. The method according to any of the claims 1 to 13, characterised in that prior to the assembling of the two substrates 1, 2, a weakened zone 5 is formed within the first substrate 1; this zone 5 defining a thin active layer

10 of a section 100 of the substrate, the thinning of the first substrate 1 being realised by detaching the section 100 along said weakened zone 5.

15. The method according to any of the claims 1 to 14, characterised in that prior to assembling, at least one of the two substrates 1, 2 including the insulating layer 3, 4 is subjected to thermal treatment intended to improve the electrical and/or physical properties of the insulating layer 3, 4.

16. The method according to claim 14, characterised in that the section 100 is used as a first substrate 1 following detachment of the thin active layer for at least two further layer transfers.