What is claimed is:

CLAIMS

1. A method for fabricating a semiconductor device comprising:

providing a substrate;

providing a gate stack on the substrate;

performing a halo implant, the halo implant forming a halo region in the substrate adjacent to opposing sides of the gate stack, the halo region comprising:

a crystalline upper vacancy rich region having excess vacancies;

a lower buried amorphous region;

forming a first diffusion region overlapping both the upper vacancy rich region and the lower buried amorphous region;

recrystallizing the buried amorphous region; and

activating dopants in the first diffusion region wherein the excess vacancies in the vacancy rich region improve the electrical activation of the first diffusion region.

2. The method of claim 1, wherein during the halo implant dopants are injected into the substrate at an angle to an axis transverse to the surface of the substrate.

3. The method of claim 1, wherein the first diffusion region has a dopant concentration that varies with depth from the surface of the substrate, the maximum dopant concentration being located at a depth Rpd from the surface of the substrate; and

the vacancy rich region has a depth that is greater than or equal to Rpd.

4. The method of claim 3, wherein the vacancy rich region has a depth of about Rpd to 3 Rpd.

5. The method of claim 3, wherein the vacancy rich region has a depth of about Rpd to 2 S_σ, S_σ being the depth where the dopant concentration drops to $1/e^{0.5}$ of the maximum dopant concentration.

6. The method of claim 1, wherein the vacancy rich region has a depth of about 1 to 10 nanometers.

7. The method of claim 1, wherein forming the halo region comprises implanting dopants at an angle of 30 to 40 degrees to the axis transverse to the surface of the substrate.

8. The method of claim 1, wherein forming the halo region comprises implanting dopants at a dose of about 5E13 to 4.5E14 atoms/cm^2.

9. The method of claim 1, wherein forming the halo region comprises implanting dopants at a dose that is less than a dose used in forming the first diffusion region.

10. The method of claim 1, wherein forming the halo region comprises implanting ions of Phosphorus or Arsenic.

11. The method of claim 1, wherein forming the halo region comprises implanting ions of Indium or Gallium.

12. The method of claim 1, wherein the first diffusion region is formed by ion implantation.

13. The method of claim 1, wherein the substrate comprises an insulating region, the halo region and first diffusion region being located above the insulating region.

14. The method of claim 13, wherein the buried amorphous region abuts the insulating region.

15. The method of claim 13, wherein the insulating region is a buried nitride or buried oxide layer.

16. The method of claim 1, further comprising forming one or more spacers adjacent to sidewalls of the gate stack; and

forming a second diffusion region on opposing sides of the gate stack after forming the spacers.

17. The method of claim 16, wherein forming the spacers comprises depositing a blanket insulating layer and etching the insulating layer, the annealing occurring during the depositing of the blanket insulating layer.

18. A method for fabricating a semiconductor device comprising:

providing a substrate;

providing a gate stack on the substrate;

performing a halo implant where dopants are injected into the substrate at an angle to an axis transverse to the surface of the substrate, the halo implant forming a halo region in the substrate adjacent to opposing sides of the gate stack, the halo region comprising:

a crystalline upper vacancy rich region that having excess vacancies;

a lower buried amorphous region;

forming a source/drain extension region substantially within each of the halo regions;

annealing the substrate to activate the dopants in the first diffusion region and recrystallize the buried amorphous region, wherein the excess vacancies in the vacancy rich region improve the electrical activation of the first diffusion region.

19. The method of claim 18, wherein the source/drain extension region has a dopant concentration that varies with depth from the surface of the substrate, the maximum dopant concentration being located at a depth Rpd from the surface of the substrate; and

the vacancy rich region has a depth that is greater than or equal to Rpd.

20. The method of claim 19, further comprising forming one or more spacers adjacent to sidewalls of the gate stack; and

forming a source/drain region on opposing sides of the gate stack after forming the spacers.

21. A transistor comprising:

a gate stack disposed above the surface of a substrate;

halo regions in the substrate on opposing sides of the gate stack, the halo region at an initial stage comprises upper and lower regions, the upper region comprises a crystalline region having excess vacancies and the lower region comprises an amorphous region; and

source/drain diffusion regions disposed in the halo regions adjacent to the gate stack, the source/drain diffusion regions comprise a depth which is below an interface of the upper and lower regions, wherein the upper region reduces transient enhanced diffusion.

What is claimed is

CLAIMS

1. A method for forming a device comprising:

providing a substrate;

implanting first type dopants in the substrate to form a first doped region, wherein the first doped region as formed includes

a crystalline vacancy rich region, and

a buried amorphous region, wherein the vacancy rich region extends from the surface of the substrate to a top of the buried amorphous region;

implanting second type dopants having a second polarity into the substrate to form a second doped region, wherein the second doped region is contained within the first doped region and overlaps both the vacancy rich and buried amorphous regions, and a peak second dopant concentration is located at a depth Rpd from the surface of the substrate, wherein the vacancy rich region has a depth that is greater than or equal to Rpd;

recrystallizing the buried amorphous regions; and

activating the second type dopants in the second doped region, wherein the crystalline upper vacancy rich region has a sufficient amount of excess vacancies to improve electrical activation in the second doped region above the solid solubility limit.

2. The method in claim 1 wherein the first doped region comprises a halo region.

3. The method in claim 1 wherein the second doped region comprises a diffusion region.

4. The method in claim 1 wherein implanting the first type dopants comprising injecting dopants into the substrate at angle to an axis transverse to the surface of the substrate.

5. The method in claim 1 wherein the vacancy rich region has a depth of about Rpd to 3 Rpd.

6. The method in claim 1 wherein the vacancy rich region has a depth of about Rpd to 2 S_{σ}, S_{σ} being the depth where the dopant concentration drops to $1/e^{0.5}$ of the maximum dopant concentration.

7. The method in claim 1 wherein the vacancy rich region has a depth of about 1 to 10 nanometers.

8. A method for forming a device comprising:

providing a substrate;

implanting first type dopants in the substrate to form a first doped region, wherein the first doped region as formed includes

a crystalline vacancy rich region, and

a buried amorphous region, wherein the vacancy rich region extends from the surface of the substrate to a top of the buried amorphous region;

implanting second type dopants having a second polarity into the substrate to form a second doped region, wherein the second doped region overlaps both the vacancy rich and buried amorphous regions;

activating the second type dopants in the second doped region, wherein the crystalline upper vacancy rich region has a sufficient amount of excess vacancies to improve electrical activation in the second doped region above the solid solubility limit.

9. The method in claim 8 wherein implanting the first type dopants in the substrate comprises forming first doped regions adjacent to a gate stack on the substrate.

10. The method in claim 9 wherein the first doped regions are isolated from each other by a portion of the substrate under the gate stack.

11. The method in claim 10 wherein implanting the second type dopants into the substrate comprises forming second doped regions which are contained within the first doped regions.

12. The method in claim 11 wherein implanting the first type dopants comprises implanting dopants at a dose that is less than a dose used in forming the second doped regions.

13. The method in claim 8 wherein the second type dopants comprise a peak concentration located at a depth Rpd from the surface of the substrate, wherein the vacancy rich region has a depth that is greater than or equal to Rpd.

14. The method in claim 11 wherein the substrate comprises a buried insulating region, the first and second doped regions being located above the insulating region.

15. The method in claim 14 wherein the buried amorphous region abuts the buried insulating region.

16. The method in claim 14 wherein the buried insulating region is a buried nitride or buried oxide layer.

17. The method in claim 8 wherein:

the substrate comprises a crystalline on insulator substrate having a crystalline surface substrate separated by a crystalline bulk substrate by an insulator layer;

the first doped regions extend below the insulator layer into the bulk substrate, wherein

the crystalline upper vacancy rich region is disposed in the surface substrate, and

the lower buried amorphous region extends from the surface substrate into the bulk substrate; and

the second doped regions are disposed in the surface substrate.

18. The method in claim 8 wherein the first doped region comprises a halo region.

19. The method in claim 8 wherein the second doped region comprises a diffusion region.

20. A method for forming a device comprising:

providing a substrate having a buried insulating region;

implanting first type dopants in the substrate to form a first doped region, wherein the first doped region as formed includes

a crystalline vacancy rich region, and

a buried amorphous region, wherein the vacancy rich region extends from the surface of the substrate to a top of the buried amorphous region;

implanting second type dopants having a second polarity into the substrate to form a second doped region, wherein the second doped region overlaps both the vacancy rich and buried amorphous regions;

activating the second type dopants in the second doped region, wherein the crystalline upper vacancy rich region has a sufficient amount of excess vacancies to improve electrical activation in the second doped region above the solid solubility limit.