

## Description

### BACKGROUND OF THE INVENTION

#### Field of the invention

The present invention relates generally to radio receivers and, more particularly, is directed to electronic apparatus having a synthesizer-type receiver which is preferably combined with a cassette type tape player and/or a compact disk (CD) player in a unitary assembly.

### DESCRIPTION OF THE PRIOR ART

It is known to provide, in a unitary assembly, an AM/FM radio receiver with a cassette tape player and/or a CD player, and in which the AM/FM receiver, the cassette tape player and the CD player are independently controlled by respective micro-computers.

It is also known to employ an AM/FM receiver of the synthesizer-type in such unitary assembly. For example, as shown in Fig. 1, a known electronic apparatus comprises, in a unitary assembly, an AM/FM receiving section 1 of the synthesizer-type, a CD player section 2, a cassette tape player or deck section 3, a main or master micro-computer 10, slave micro-computers 11, 12 and 13 for controlling the AM/FM receiver section 1, the CD player section 2 and the cassette tape player section 3, respectively, and an additional slave micro-computer 14 for processing control signals supplied from or to a remote control receiver 15 and transmitted from or to a remote commander (not shown). The AM/FM receiver section 1 of the synthesizer-type conventionally includes a phase locked loop (PLL) in which a frequency-dividing ratio signal from the micro-computer 11 determines the dividing ratio of a variable frequency-dividing circuit (not shown) in the PLL and thereby determines the receiving frequency of the receiver section 1.

The micro-computers 11-14 may each be constituted by a 4-bit single chip-type micro-computer, and are all controlled or commanded by the main computer 10. When the operations of the receiver section 1, the CD player section 2, the tape cassette player section 3 and the remote control receiver 15 are controlled by the micro-computers 11, 12, 13, 14, respectively, and such micro-computers 11-14 are controlled by the main micro-computer 10, the software programs in the micro-computers 11-14 can be easily developed so as to enable the sections 1, 2 and 3 to perform numerous operations and functions. In a practical example of the prior art arrangement illustrated in Fig. 1, the main micro-computer 10 is a micro-processor obtainable from the NEC Corporation under the designation D 7532B4GC, the micro-computer 11 is a micro-processor also obtainable from the NEC Corporation under the designation D 1725G, the micro-computer 12 is obtainable from Sony Corporation under the designation CXP 507B, the micro-computer 13 is also obtainable from Sony Corpora-

tion under the designation CXP 5024, and the micro-computer 14 is obtainable from Mitsubishi Electric Corporation under the designation M 50920.

It will be appreciated that a clock signal is required for operation of each of the micro-computers 10-14. If the clock signal CK for the main micro-computer 10 has a relatively high clock frequency  $f_c$ , for example, of 4.2 MHz, then as shown in Fig. 2A, higher harmonic components  $Sh$  of the clock signal CK are distributed within the FM broadcasting frequency band of 76 to 108 MHz. As a result, when the receiver section 1 is operative to receive a FM signal broadcast at a frequency that is equal to one of the higher harmonics  $Sh$  of the clock frequency  $f_c$ , the reception of such broadcast signal is disturbed.

In order to avoid the above problem, it has been suggested, for example, as shown on Fig. 2B, that the frequency  $f_c$  of the clock signal CK be decreased to approximately the lowest frequency at which the main computer 10 can be operated, for example, to a frequency of 400 kHz, so that the order of the higher harmonic components  $Sh$  of the clock signal CK distributed within the FM broadcasting band is substantially higher than the order of the higher harmonic components within the FM broadcasting band in Fig. 2A. By reason of the foregoing, when the frequency  $f_c$  of the clock signal CK of the main micro-computer 10 is decreased to about 400 kHz, the level of the higher harmonic components  $Sh$  of such clock signal within the FM broadcasting band is so small as to be negligible. More specifically, in the case illustrated in Fig. 2A, the higher harmonic components  $Sh$  of the clock signal CK distributed in the FM broadcasting band when the clock frequency  $f_c$  is 4.2 MHz are in the range from the 19th order to the 24th order, and at least some of the levels thereof are of sufficient magnitude to produce the undesired disturbance of the FM reception. On the other hand, in the case illustrated in Fig. 2B, and in which the frequency  $f_c$  of the clock signal CK is decreased to 400 kHz, the higher harmonic components  $Sh$  of the clock signal CK distributed within the FM broadcasting band are from the 190th order to the 270th order. When the higher harmonic components  $Sh$  of the clock signal CK within the FM broadcasting band range from the 190th order to the 270th order, the levels of such higher harmonic components are, as shown, so small as to be satisfactorily neglected and to ensure that reception of the FM broadcast signal will be undisturbed. When the frequency of the clock signal CK for the main computer 10 is reduced as described above, for avoiding disturbance of the reception of the FM broadcast signal by the higher harmonic components of such clock signal, the frequencies of the clock signals employed in the micro-computers 11-14 will be similarly decreased for the same reason.

Of course, if low clock frequencies are used in the micro-computers 10-14, as described above, the processing speeds of the micro-computers 10-14 are correspondingly lowered. Since the micro-computers 11-14 are employed for independently controlling the re-

spective sections 1, 2 and 3 and remote control receiver 15, such computers do not need to operate at high speed. Therefore, the clock frequencies of the micro-computers 11-14 can be reduced, as described above, to ensure that the higher harmonic components of the clock signals employed in the micro-computers 11-14 have negligible levels.

However, the main micro-computer 10 exerts overall system control of the electronic apparatus and the micro-computers 11-14 are, in turn, operated under the control of the main micro-computer 10 so that, if the frequency  $f_c$  of the clock signal CK of the main micro-computer 10 is lowered, for example, to 400 kHz, as described above, the correspondingly lowered processing speed of the main micro-computer 10 reduces the range of operations of the receiver section 1, the CD player section 2, the tape cassette player section 3 and the remote control receiver 15 controlled by the main computer. For example, in the case where audio levels are displayed, the reduced processing speed of the main micro-computer 10 will introduce a time delay in the audio level display. Thus, the audio level indication will not correspond to real time conditions.

Patent Abstracts of Japan, vol. 12 No 261 (E636) and JP-A-6346829 disclose a clock generating circuit in which a clock signal frequency is deviated so as to avoid invasion of clock signal harmonics into a received channel.

Furthermore, GB 2194 696 discloses an electronic apparatus having clock generating means including means for shifting the frequency of the clock signal when a selected receiving frequency is disturbed by a higher harmonic component of the clock signal. Thus, GB 2 194 696 discloses an apparatus in accordance with the preamble of claim 1.

## **OBJECTS AND SUMMARY OF THE INVENTION**

Accordingly, it is an object of the present invention to provide an electronic apparatus which includes a synthesizer-type receiver, and which eliminates the above mentioned Problems and disadvantages inherent in the prior art.

More specifically, it is an object of the present invention to provide an electronic apparatus including a synthesizer-type receiver which can prevent disturbance of the reception of an FM broadcast signal by higher harmonic components of a clock signal employed in a micro-computer for controlling the receiver.

It is another object of the present invention to provide an electronic apparatus including a synthesizer-type receiver, as aforesaid, and which further includes a CD player and/or a cassette tape player in a unitary assembly therewith.

It is still another object of the present invention to provide an electronic apparatus including a synthesizer-type receiver, as aforesaid, controlled by a micro-computer, and in which disturbance of the reception

of FM broadcast signals by higher harmonic components of a clock signal for operating the micro-computer is avoided without reducing the clock frequency to an extent that would unduly limit the operations of the apparatus controllable by the micro-computer.

It is a further object of the present invention to provide an electronic apparatus including a synthesizer-type receiver, as aforesaid, and which can be produced at relatively low cost.

According to the invention, there is provided an electronic apparatus comprising:

a receiver having a synthesizer section for selecting a receiving frequency and receiving a signal broadcast at the selected receiving frequency, and means providing an information signal corresponding to said selected receiving frequency;  
control means operable on the basis of a clock signal for controlling operation of at least said synthesizer section of the receiver; and  
clock generating means for providing said clock signal including means responsive to said information signal for shifting the frequency of said clock signal when said selected receiving frequency is a frequency disturbed by a higher harmonic component of said clock signal or a frequency-divided version of said clock signal, in which the amount of the frequency shift  $\Delta f = f_c / 2n$ , where  $f_c$  is the frequency of the clock signal and  $n$  is the average of the orders of the higher harmonic components of the clock signal within the frequency band of the broadcast signals.

The frequency shift of the clock signal according to the invention is such that the higher harmonic components of the shifted clock signal in the frequency band are located midway between the higher harmonic components of the original clock signal.

The above, and other objects, features and advantages of the present invention, will be apparent in the following detailed description of a preferred embodiment of the invention which is to be read in conjunction with the accompanying drawings forming a part thereof, and in which corresponding parts or components are identified by the same reference numerals in the several views of the drawings.

## **BRIEF DESCRIPTION OF THE DRAWINGS**

Fig. 1 is a schematic block diagram of an electronic apparatus according to the prior art which includes a synthesizer-type AM/FM receiver along with a CD player and a cassette tape player in a unitary assembly capable of remote control;

Figs. 2A and 2B are graphs of frequency characteristics to which reference is made in explaining problems encountered with the electronic apparatus of Fig. 1 and a modification thereof;

Fig. 3 is a schematic block diagram showing an electronic apparatus similar to that of Fig. 1, but incorporating an embodiment of the present invention; and

Figs. 4A and 4B are graphs of frequency characteristics to which reference will be made in explaining the operation of the embodiment of the invention illustrated in Fig. 3.

### DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

Referring now to Fig. 3, it will be seen that many parts of the electronic apparatus embodying the present invention, as there illustrated, are identified by the same reference numerals as were used to identify the corresponding parts in the apparatus of Fig. 1 and will not be again described in detail.

In the embodiment of the invention illustrated in Fig. 3, the main or master micro-computer 10 has a clock oscillator circuit by which the clock signal for the master computer 10 is generated, for example, with a frequency  $f_c$  of 4.2 MHz. Such clock oscillator circuit for the master micro-computer 10 is shown to have a ceramic oscillator 20 for oscillating a clock signal which is connected between clock terminals  $\sigma_1$  and  $\sigma_2$  of the main micro-computer 10, and capacitors 21 and 22 respectively connected between clock terminal  $\sigma_1$  and ground and between clock terminal  $\sigma_2$  and ground. Further, in accordance with the illustrated embodiment of the invention, a capacitor 23 and a collector-emitter path of an npn transistor 24 are connected in series between the clock terminal  $\sigma_2$  and ground.

The oscillation frequency  $f_c$  of the ceramic oscillator is selected to achieve a suitably high processing speed of the main micro-computer 10, for example, the oscillation frequency of the ceramic oscillator 20 is selected to be 4.2 MHz. When the transistor 24 is turned ON, the capacitor 23 is connected in parallel with the capacitor 22 whereby the clock frequency  $f_c$  of the main micro-computer 10 is shifted by an amount  $\Delta f$  in the lower direction. The amount  $\Delta f$  that the clock frequency  $f_c$  is shifted when the transistor 24 is turned ON is determined as follows:

If it is assumed that  $n$  represents the order of the higher harmonic component  $Sh$  of the clock frequency  $f_c$  which is situated in the FM broadcasting band, then a frequency  $f_i$  centered between the frequency of the  $(n-1)$ th higher harmonic component  $Sh$  and the frequency of the  $n$ th order higher harmonic component  $Sh$  can be expressed as in the below equation (1):

$$f_i = (n - 1/2) f_c \quad (1)$$

Accordingly, the frequency  $f_s$  of a fundamental wave signal of which the frequency  $f_i$  is the  $n$ th order higher harmonic component can be expressed as:

$$f_s = f_i/n$$

or

$$f_s = f_c - f_c/(2n) \quad (2)$$

The difference between the frequency  $f_s$  and the clock frequency  $f_c$  represents the amount of the frequency shift  $\Delta f$ , and is expressed as:

$$\Delta f = f_c - f_s$$

$$\Delta f = f_c/(2n) \quad (3)$$

In other words, if the amount of the frequency shift  $\Delta f$  is selected in accordance with equation (3) above, then the higher harmonic components  $Sh'$  of the shifted clock frequency  $f_s$  (indicated in dash lines on Fig. 4A) are located midway between the higher harmonic components  $Sh$  of the original clock frequency  $f_c$  (shown in solid lines in Fig. 4A).

If, for example, the higher harmonic components  $Sh$  of the original frequency  $f_c$  that lie within the FM broadcasting band range from the 19th order harmonic component to the 25th order harmonic component, that is,  $n = 19$  to 25, an average value of  $n$ , that is,  $n = 22$ , may be adopted for the sake of simplicity in determining the value of  $\Delta f$ . Substituting  $n = 22$  in the above equation (3) yields:

$$\Delta f = f_c/(2 \times 22) = f_c/44$$

In other words, when  $f_c = 4.2$  MHz, then  $\Delta f$  approximately equals 95 kHz.

Therefore, in the embodiment of the present invention being here described, the capacitance of the capacitor 23 is selected so that, when the transistor 24 is turned ON, the frequency of the clock signal is shifted downwardly by the amount  $\Delta f = 95$  kHz.

Further, in the electronic apparatus according to this invention, as illustrated in Fig. 3, the micro-computer 11 associated with the synthesizer-type AM/FM receiver 1 is operative to provide an information signal  $S_f$  (Fig. 4B) which is related to the receiving frequency  $f_r$  selected by the synthesizer-type receiver 1 as will now be described.

More specifically, the signals  $S_f$  from the micro-computer 11 is at the high level "1" so long as the selected receiving frequency  $f_r$  satisfies the below inequality:

$$n(f_c - \Delta f/2) < f_r < n(f_c + \Delta f/2) \quad (4)$$

At all other times, that is, whenever the selected receiving frequency  $f_r$  does not satisfy the inequality (4), the signal  $S_f$  is at the low level "0".

Since the micro-computer 11 provides to the synthesizer-type receiver 1 the frequency-dividing ratio for determining the selected receiving frequency  $f_r$  of the receiver, the micro-computer 11 can readily determine whether or not the frequency-dividing ratio corresponds to the inequality (4) and provide the signal  $S_f$  accordingly.

Finally, as shown in Fig. 3, the signal  $S_f$  from the micro-computer 11 is applied to the base of the transistor 24 so that the latter is turned ON when the signal  $S_f$  is "1" for shifting the clock frequency  $f_c$  by the amount  $\Delta f$ , whereas, at all other times, that is, so long as the signal  $S_f$  is "0", the clock frequency remains at its normal value  $f_c$ .

It will be appreciated that, when an FM broadcast

signal is received at a selected receiving frequency  $f_r$  which does not satisfy the inequality (4), so that the information signal  $S_f$  is "0" and the transistor 24 is turned OFF with the result that the clock frequency  $f_c$  of the main micro-computer 10 is maintained at the original frequency of 4.2 MHz, the higher harmonic components  $Sh$  of the clock signal CK do not disturb the reception of such FM broadcast signal.

On the other hand, when an FM broadcast signal is received with a selected receiving frequency  $f_r$  which satisfies the inequality (4), so that  $S_f$  is "1" and the transistor 24 is turned ON, the capacitor 23 is thereby connected in parallel with the capacitor 22 with the result that the clock frequency  $f_c$  of the main micro-computer 10 is shifted downwardly from the original frequency 4.2 MHz by the amount  $\Delta f = 95$  kHz to the lower frequency  $f_s$ .

When the clock frequency  $f_s$  is determined as described above, then the higher harmonic components  $Sh'$  thereof (shown in dotted lines on Fig. 4A) are shifted from the frequency  $n \cdot f_c$  (MHz) of the higher harmonic components  $Sh$  (shown by solid lines) of the original clock signal CK by the frequency  $n \cdot \Delta f$  (kHz) with the result that the shifted higher harmonic components  $Sh'$  do not disturb the FM broadcast signal being received at that time.

It will be appreciated from the above that, in accordance with the present invention, when an FM broadcast signal is received by the synthesizer-type receiver 1, the clock frequency  $f_c$  of the master micro-computer 10 is shifted when required in response to the selected receiving frequency  $f_r$  so that the reception of the FM broadcast signal will not, in any case, be disturbed by the higher harmonic components of the clock signal CK. Furthermore, since the clock frequency  $f_c$  of the master micro-computer 10 is either the original frequency of 4.2 MHz or is equal to that frequency reduced by 95 kHz, it will be appreciated that the master micro-computer 10 is operating, at all times, with a clock of substantially high frequency, and thus can perform the necessary processing at a sufficiently high speed. Therefore, the illustrated electronic apparatus comprising an AM/FM receiver 1, a CD player 2 and a tape cassette player 3 can be operated in a wide variety of operating modes under the control of the master micro-computer 10.

If an error exists in the ceramic oscillator 20 or in the capacitors 21 and 22 so that the clock frequency  $f_c$  deviates from the desired value of 4.2 MHz, there is a similar variation or deviation of the frequencies of the higher harmonic components  $Sh$  of the clock frequency. However, in accordance with the present invention, when the clock frequency  $f_c$  is shifted by the amount  $\Delta f$ , the higher harmonic components  $Sh'$  of the shifted clock frequency  $f_s$  are each situated substantially midway between adjacent higher harmonic components  $Sh$  (shown by the solid lines on Fig. 4A) of the original clock frequency  $f_c$ . Thus, even if the clock frequency  $f_c$  fluctuates or deviates, when an FM broadcast signal is received at the selected receiving frequency  $f_r$  which is situated, in the FM

broadcast band, adjacent one of the higher harmonic components  $Sh$ , the shift of the clock frequency by the amount  $\Delta f$  will still result in the shifted higher harmonic components  $Sh'$  being substantially spaced from the receiving frequency  $f_r$  so that the FM broadcast signal will not be disturbed by the higher harmonic components  $Sh'$ .

It will be appreciated that the present invention, as described above, involves only the addition of the capacitor 23 and the npn transistor 24 to the clock oscillator circuit and a suitable modification of a portion of the program of the micro-computer 11 for operating in the described manner so as to ensure that higher harmonics of the clock frequency will not disturb the received FM broadcast signal. Therefore, a synthesizer-type receiver having the described advantages of the present invention can be provided at little extra cost.

Although the previously described embodiment of the invention is intended to avoid disturbance of the received FM broadcast signal by the higher harmonic components  $Sh$  of the clock signal CK itself having the clock frequency  $f_c$ , the invention can be similarly applied to avoiding disturbance of an FM broadcast signal by higher harmonic components of a frequency divided pulse signal having a frequency of 2.1 MHz, and which results from frequency-dividing by two the clock signal CK within the main micro-computer 10. In such case, as before, the clock frequency  $f_c$  is shifted in response to the receiving frequency  $f_r$  being near to a higher harmonic component of the frequency-divided pulse signal, with the result that such higher harmonic component of the frequency-divided pulse signal is shifted away from the receiving frequency  $f_r$ .

Further, although the present invention has been described as applied to an electronic apparatus in which a synthesizer-type AM/FM radio receiver is combined with a cassette tape player and a CD player in a unitary assembly, it will be appreciated that the invention is not limited thereto and can be similarly applied to the combination of a synthesizer-type AM/FM radio receiver with either a cassette tape player or a CD player, or merely to the synthesizer-type AM/FM radio receiver in which only one microcomputer is utilized. Furthermore, the present invention can be similarly employed in a synthesizer-type TV tuner for shifting the clock frequency  $f_c$  and thereby ensuring that higher harmonic components of the clock signal will not disturb a received broadcast television signal.

## Claims

1. An electronic apparatus comprising :

a receiver (1) having a synthesizer section for selecting a receiving frequency and receiving a signal broadcast at the selected receiving frequency, and means providing an information



signal is received at a selected receiving frequency  $f_r$  which does not satisfy the inequality (4), so that the information signal  $S_f$  is "0" and the transistor 24 is turned OFF with the result that the clock frequency  $f_c$  of the main micro-computer 10 is maintained at the original frequency of 4.2 MHz, the higher harmonic components  $Sh$  of the clock signal CK do not disturb the reception of such FM broadcast signal.

On the other hand, when an FM broadcast signal is received with a selected receiving frequency  $f_r$  which satisfies the inequality (4), so that  $S_f$  is "1" and the transistor 24 is turned ON, the capacitor 23 is thereby connected in parallel with the capacitor 22 with the result that the clock frequency  $f_c$  of the main micro-computer 10 is shifted downwardly from the original frequency 4.2 MHz by the amount  $\Delta f = 95$  kHz to the lower frequency  $f_s$ .

When the clock frequency  $f_s$  is determined as described above, then the higher harmonic components  $Sh'$  thereof (shown in dotted lines on Fig. 4A) are shifted from the frequency  $n \cdot f_c$  (MHz) of the higher harmonic components  $Sh$  (shown by solid lines) of the original clock signal CK by the frequency  $n \cdot \Delta f$  (kHz) with the result that the shifted higher harmonic components  $Sh'$  do not disturb the FM broadcast signal being received at that time.

It will be appreciated from the above that, in accordance with the present invention, when an FM broadcast signal is received by the synthesizer-type receiver 1, the clock frequency  $f_c$  of the master micro-computer 10 is shifted when required in response to the selected receiving frequency  $f_r$  so that the reception of the FM broadcast signal will not, in any case, be disturbed by the higher harmonic components of the clock signal CK. Furthermore, since the clock frequency  $f_c$  of the master micro-computer 10 is either the original frequency of 4.2 MHz or is equal to that frequency reduced by 95 kHz, it will be appreciated that the master micro-computer 10 is operating, at all times, with a clock of substantially high frequency, and thus can perform the necessary processing at a sufficiently high speed. Therefore, the illustrated electronic apparatus comprising an AM/FM receiver 1, a CD player 2 and a tape cassette player 3 can be operated in a wide variety of operating modes under the control of the master micro-computer 10.

If an error exists in the ceramic oscillator 20 or in the capacitors 21 and 22 so that the clock frequency  $f_c$  deviates from the desired value of 4.2 MHz, there is a similar variation or deviation of the frequencies of the higher harmonic components  $Sh$  of the clock frequency. However, in accordance with the present invention, when the clock frequency  $f_c$  is shifted by the amount  $\Delta f$ , the higher harmonic components  $Sh'$  of the shifted clock frequency  $f_s$  are each situated substantially midway between adjacent higher harmonic components  $Sh$  (shown by the solid lines on Fig. 4A) of the original clock frequency  $f_c$ . Thus, even if the clock frequency  $f_c$  fluctuates or deviates, when an FM broadcast signal is received at the selected receiving frequency  $f_r$  which is situated, in the FM

broadcast band, adjacent one of the higher harmonic components  $Sh$ , the shift of the clock frequency by the amount  $\Delta f$  will still result in the shifted higher harmonic components  $Sh'$  being substantially spaced from the receiving frequency  $f_r$  so that the FM broadcast signal will not be disturbed by the higher harmonic components  $Sh'$ .

It will be appreciated that the present invention, as described above, involves only the addition of the capacitor 23 and the npn transistor 24 to the clock oscillator circuit and a suitable modification of a portion of the program of the micro-computer 11 for operating in the described manner so as to ensure that higher harmonics of the clock frequency will not disturb the received FM broadcast signal. Therefore, a synthesizer-type receiver having the described advantages of the present invention can be provided at little extra cost.

Although the previously described embodiment of the invention is intended to avoid disturbance of the received FM broadcast signal by the higher harmonic components  $Sh$  of the clock signal CK itself having the clock frequency  $f_c$ , the invention can be similarly applied to avoiding disturbance of an FM broadcast signal by higher harmonic components of a frequency divided pulse signal having a frequency of 2.1 MHz, and which results from frequency-dividing by two the clock signal CK within the main micro-computer 10. In such case, as before, the clock frequency  $f_c$  is shifted in response to the receiving frequency  $f_r$  being near to a higher harmonic component of the frequency-divided pulse signal, with the result that such higher harmonic component of the frequency-divided pulse signal is shifted away from the receiving frequency  $f_r$ .

Further, although the present invention has been described as applied to an electronic apparatus in which a synthesizer-type AM/FM radio receiver is combined with a cassette tape player and a CD player in a unitary assembly, it will be appreciated that the invention is not limited thereto and can be similarly applied to the combination of a synthesizer-type AM/FM radio receiver with either a cassette tape player or a CD player, or merely to the synthesizer-type AM/FM radio receiver in which only one microcomputer is utilized. Furthermore, the present invention can be similarly employed in a synthesizer-type TV tuner for shifting the clock frequency  $f_c$  and thereby ensuring that higher harmonic components of the clock signal will not disturb a received broadcast television signal.

## Claims

### 1. An electronic apparatus comprising:

a receiver (1) having a synthesizer section for selecting a receiving frequency and receiving a signal broadcast at the selected receiving frequency, and means providing an information



signal (Sf) corresponding to said selected receiving frequency;  
control means (10) operable on the basis of a clock signal (CK) for controlling operation of at least said synthesizer section of the receiver (1); and

clock generating means for providing said clock signal (CK) including means responsive to said information signal (Sf) for shifting the frequency (fc) of said clock signal (CK) when said selected receiving frequency is a frequency disturbed by a higher harmonic component of said clock signal (CK) or a frequency-divided version of said clock signal, characterized in that the amount of the frequency shift  $\Delta f = fc/2n$  where fc is the frequency of the clock signal and n is the average of the orders of the higher harmonic components of the clock signal within the frequency band of the broadcast signals.

2. An electronic apparatus as claimed in claim 1, further comprising at least one additional section (2, 3, 15) controllable by said control means (10) on the basis of said clock signal (CK) and being selected from compact disc player means (2), cassette tape player means (3) and remote control means (15).
3. An electronic apparatus as claimed in claim 2, in which said control means (10) is a micro-computer.
4. An electronic apparatus as claimed in claim 1, in which said clock generating means includes an oscillator (20) having a predetermined oscillating frequency (fc) to which said frequency of the clock signal (CK) corresponds, and said means for shifting said frequency of the clock signal.
5. An electronic apparatus as claimed in claim 4, in which said oscillator is connected between clock terminals ( $\phi 1$ ,  $\phi 2$ ), the clock generating means further comprising first and second capacitors (21, 22) connected between said terminals ( $\phi 1$ ,  $\phi 2$ ) and ground, and said means for shifting the frequency of the clock signal includes a third capacitor (23) connected from one ( $\phi 2$ ) of said clock terminals to ground through a transistor (24) which is turned ON by said information signal (Sf).
6. An electronic apparatus as in claim 5, in which said transistor (24) is an npn transistor having a collector-emitter path to which said third capacitor (23) is connected, said information signal (Sf) being connected to the base of said transistor to turn ON the transistor only when said information signal (Sf) is at a high level, said information signal being at said high level only when shifting of the clock signal is operative.

7. An electronic apparatus as claimed in any of claims 1 to 6, in which said means for shifting the frequency of the clock signal by said amount  $\Delta f$  is operative when the selected receiving frequency fr satisfies the below inequality:

$$n (fc - \Delta f/2) < fr < n (fc + \Delta f/2).$$

## 10 Patentansprüche

### 1. Elektronisches Gerät mit

einem Empfänger (1), der einen Synthesizerabschnitt zur Auswahl einer Empfangsfrequenz und zum Empfang eines auf der ausgewählten Empfangsfrequenz gesendeten Signals sowie Mittel zur Erzeugung eines der ausgewählten Empfangsfrequenz entsprechenden Informationssignals (Sf) aufweist,

einer auf der Basis eines Taktsignals (CK) betreibbaren Steuereinrichtung (10) zur Steuerung der Funktion zumindest des Synthesizerabschnitts des Empfängers (1) und

einer Taktgeneratoreinrichtung zur Erzeugung des Taktsignals (CK) mit auf das genannte Informationssignal (Sf) ansprechenden Mitteln zur Verschiebung der Frequenz (fc) des Taktsignals (CK), wenn die ausgewählte Empfangsfrequenz eine Frequenz ist, die durch eine höhere harmonische Komponente des Taktsignals (CK) oder eine frequenzgeteilte Version des Taktsignals (CK) gestört wird,

**dadurch gekennzeichnet,**  
daß die Größe der Frequenzverschiebung  $\Delta f = fc/2n$  ist, wobei fc die Frequenz des Taktsignals und n der Mittelwert der Ordnungen der höheren harmonischen Komponenten des Taktsignals innerhalb des Frequenzbands der Rundfunksignale bedeuten.

2. Elektronisches Gerät nach Anspruch 1 ferner mit wenigstens einem Zusatzteil (2, 3, 15), das von der Steuereinrichtung (10) auf der Basis des Taktsignals (CK) steuerbar ist und aus der Gruppe von Teilen ausgewählt ist, die einen CD-Player (2), einen Kassettenrekorder (3) und eine Fernsteuerung (15) umfaßt.

3. Elektronisches Gerät nach Anspruch 2, bei dem die Steuereinrichtung (10) ein Mikrocomputer ist.

4. Elektronisches Gerät nach Anspruch 1, bei dem die Taktgeneratoreinrichtung einen Oszillator (20) mit einer vorbestimmten Schwingungsfrequenz (fc), dem die Frequenz des Taktsignals (CK) entspricht, sowie die Mittel zur Verschiebung der Frequenz des Taktsignals enthält.



# 5. Elektronisches Gerät nach Anspruch 4, bei dem

der Oszillator (20) zwischen Taktanschlüssen ( $\phi_1$ ,  $\phi_2$ ) angeordnet ist, die Taktgeneratoreinrichtung ferner einen ersten und einen zweiten Kondensator (21 bzw. 22) aufweist, die zwischen den Taktanschlüssen ( $\phi_1$ ,  $\phi_2$ ) und Masse angeordnet sind, und die Mittel zur Verschiebung der Frequenz des Taktsignals einen dritten Kondensator (23) umfassen, der von einem ( $\phi_2$ ) der Taktanschlüsse über einen Transistor (24), der von dem Informationssignal (Sf) in seinen leitenden Zustand steuerbar ist, mit Masse verbunden ist.

# 6. Elektronisches Gerät nach Anspruch 5, bei dem

der Transistor (24) ein pnp-Transistor ist, der eine Kollektor-Emitterstrecke besitzt, mit der der dritte Kondensator (23) verbunden ist, das Informationssignal (Sf) an der Basis des Transistors anliegt, so daß es den Transistor nur dann in seinen leitenden Zustand steuert, wenn es auf hohem Pegel liegt, und das Informationssignal nur dann auf hohem Pegel liegt, wenn die Frequenzverschiebung des Taktsignals wirksam ist.

# 7. Elektronisches Gerät nach einem der Ansprüche 1 bis 6, bei dem die Mittel zur Verschiebung der Frequenz des Taktsignals um die genannte Größe wirksam ist, wenn die ausgewählte Empfangsfrequenz fr die folgende Ungleichung erfüllt:

$$\underline{n} (fc - \Delta f/2) < fr < \underline{n} (fc + \Delta f/2).$$

## Revendications

### 1. Appareil électronique comprenant :

un récepteur (1) possédant une section synthétiseur servant à sélectionner une fréquence de réception et recevant, à la fréquence de réception sélectionnée, un signal diffusé, et un moyen produisant un signal d'information (Sf) qui correspond à ladite fréquence de réception sélectionnée ;  
un moyen de commande (10) pouvant fonctionner sur la base d'un signal d'horloge (CK) pour commander le fonctionnement d'au moins ladite section synthétiseur du récepteur (1) ; et  
un moyen générateur de signal d'horloge servant à produire ledit signal d'horloge (CK) et comportant un moyen qui répond audit signal d'information (Sf) en décalant la fréquence (fc) dudit signal d'horloge (CK) lorsque ladite fréquence de réception sélectionnée est une fré-

quence qui est perturbée par une composante harmonique supérieure dudit signal d'horloge (CK) ou d'une version divisée en fréquence de ce signal d'horloge, caractérisé en ce que la grandeur du décalage de fréquence est  $\Delta f = fc/2n$ , où fc est la fréquence du signal d'horloge et  $\underline{n}$  est la moyenne des ordres des composantes harmoniques supérieures du signal d'horloge à l'intérieur de la bande de fréquence des signaux diffusés.

2. Appareil électronique selon la revendication 1, comprenant en outre au moins une section supplémentaire (2, 3, 15) qui peut être commandée par ledit moyen de commande (10) sur la base dudit signal d'horloge (CK) et qui sera choisie parmi un moyen (2) lecteur de disque audionumérique, un moyen (3) lecteur de bande sur cassette et un moyen de télécommande (15).

3. Appareil électronique selon la revendication 2, dans lequel ledit moyen de commande (10) est un micro-ordinateur.

4. Appareil électronique selon la revendication 1, dans lequel ledit moyen générateur de signal d'horloge comporte un oscillateur (20) possédant une fréquence d'oscillation prédéterminée (fc) à laquelle correspond ladite fréquence du signal d'horloge (CK), ainsi que ledit moyen servant à décaler ladite fréquence du signal d'horloge.

5. Appareil électronique selon la revendication 4, dans lequel ledit oscillateur est connecté entre des bornes d'horloge ( $\phi_1$ ,  $\phi_2$ ), le moyen générateur de signal d'horloge comprenant en outre des premier et deuxième condensateurs (21, 22) connectés entre lesdites bornes ( $\phi_1$ ,  $\phi_2$ ) et la terre, et ledit moyen de décalage de la fréquence du signal d'horloge comporte un troisième condensateur (23) connecté entre l'une ( $\phi_2$ ) desdites bornes d'horloge et la terre via un transistor (24) qui commute dans l'état conducteur sous l'action dudit signal d'information (Sf).

6. Appareil électronique selon la revendication 5, dans lequel ledit transistor (24) est un transistor npn dont le trajet collecteur-émetteur est connecté audit troisième condensateur (23), ledit signal d'information (Sf) n'étant appliqué à la base dudit transistor, pour rendre conducteur le transistor, que lorsque ledit signal d'information (Sf) est à un niveau haut, ledit signal d'information n'étant audit niveau haut que lorsque le décalage du signal d'horloge est activé.

7. Appareil électronique selon l'une quelconque des revendications 1 à 6, dans lequel ledit moyen servant à décaler la fréquence du signal d'horloge de ladite quantité  $\Delta f$  est activé lorsque la fréquence de



réception sélectionnée (fr) satisfait l'inégalité  
ci-après :

$$n(fc - \Delta f/2) < fr < n(fc + \Delta f/2).$$

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