

FLASH EEPROM USING CHARGE PUMPING

Abstract of the Disclosure:

An integrated circuit arrangement for providing erase voltages to a flash EEPROM - memory array including one charge pump for generating a first high voltage with substantial current which may be used for application to the source terminals of flash EEPROM memory cells during erase and to the gate terminals of flash EEPROM memory cells during programming, and another charge pump for generating a second lower voltage which may be used for application to the drain terminals of flash EEPROM memory cells during programming.

Figure 3

This Sheet Has Been Replaced

THIS SHEET HAS BEEN
REPLACED