ABSTRACT

FORMATION OF SMALL GATES BEYOND LITHOGRAPHIC LIMITS

A method of fabricating an ultra-small semiconductor structure comprising the following steps. A substrate having a lower dielectric layer and an overlying upper dielectric layer formed thereover is provided. Using a lithography process having a lithography limit, the upper dielectric layer is patterned to form a first opening exposing a portion of the lower dielectric layer. The first opening having exposed side walls and a width equal to the lithography limit. Sidewall spacers having a lower width are formed over the exposed side walls of the first opening. Using the sidewall spacers as masks, the lower dielectric layer is patterned to form a lower opening having a width less than the first opening width. The patterned upper dielectric layer is removed. An ultra-small semiconductor structure is formed within the lower opening. The ultra-small semiconductor structure having a width equal to the lithography limit minus twice the lower width of the sidewall spacer.

FIGURE 1