

ABSTRACT

FAST INTERFACE ARRANGEMENT

An interface arrangement including the cascade connection of a differential pre-amplifier (HPA1, HPA2) and a comparator (DA), and generally known as fast Low Voltage Differential Signal [LVDS] circuit for interfacing electronic chips. The current standards for such a LVDS circuit specify a minimum switching threshold voltage for the small differential input signal, while the common mode input signal varies over a very large range, both at a very high frequency. This is achieved owing to the fact that the differential pre-amplifier comprises a first (HPA1) and a second (HPA2) half pre-amplifier, each receiving the arrangement inputs (INN, INP) in an opposite way. Each half pre-amplifier (HPA1/HPA2) having first input inverter means (NN1, PN1) coupling an input (INN/INP) to an output (OUT1/OUT2) thereof, and second input inverter means (NP1, PM1, PM2; PP1, NM1, NM2) coupling the other input (INP/INN) to the output via current mirror means (PM1, PM2; NM1, NM2). The output current of the second input inverter means is thereby inverted with respect to the output current of the first input inverter means. To obtain a controlled gain, the half pre-amplifier further includes a short-circuited inverter.

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Fig. 1