CLAIMS

What is claimed is:

1. A method of testing a semiconductor device on a wafer, the method comprising:

holding the wafer with a chuck;

contacting a first pad of the semiconductor device with a plurality of probe needles, the plurality of probe needles comprising a plurality of first needles and at least one second needle, and the plurality of probe needles comprising tips, wherein the tips of the plurality of first needles are positioned so as to provide equi-resistant paths between tips of the first needles to a nearest tip of a probe needle of the at least one second needle;

providing current through the plurality of first needles; and measuring voltage at the at least one second needle, wherein:

providing current comprises inducing a current between the first needles and the chuck along a current path through the chuck, the semiconductor device, the first pad, and tips of the plurality of first needles that are in contact with the first pad, in such order.

2. The method of claim 1, further comprising:

computing an ON resistance of the semiconductor device based on the measured voltage.

3. A method of manufacturing a semiconductor device incorporating the method of testing a claim 2, further comprising; the method of manufacturing comprising: selecting at least one subsequent step in the manufacturing based on the computed ON resistance.

4. The method of claim 2, wherein:

the method of claim 2, wherein the ON resistance is less than 1 milliOhm.

5. The method of claim 1, wherein:

the semiconductor device is a power FET.

6. The method of claim 4, wherein:

providing current comprises sourcing current through each of the plurality of first needles in the range of 0 Amps to 7 Amps.

7. The method of claim 1, wherein:

the at least one second needle comprises a single needle.

8. The method of claim 1, wherein:

the tips of the plurality of first needles are disposed equi-distant from the tips of the at least one second needle.

9. The method of claim 1, wherein:

the at least one second needle comprises a plurality of second needles; and a tip of each of the plurality of second needles is positioned adjacent a tip of the plurality of first needles.

10. The method of claim 9, wherein:

measuring voltage comprising measuring a composite voltage at a first node to which the plurality of second needles are connected.

11. The method of claim 9, wherein:

measuring voltage comprising measuring a composite voltage at a first node to which the plurality of second needles are coupled through equal-valued resistors.

12. The method of claim 1, wherein:

measuring voltage comprises measuring a voltage difference between the chuck and the at least one second needle.

13. The method of claim 1, wherein:

the semiconductor device is a first semiconductor device on a wafer;

the wafer comprises at least one second semiconductor device adjacent the first semiconductor device, each of the at least one second semiconductor device comprising a second pad;

measuring voltage comprises:

biasing on the at least one second semiconductor device; and

connecting the second pad of the at least one second semiconductor device to a second node; and

measuring a voltage difference between the second node and the at least one second needle.

14. A probe card for testing a semiconductor device on a wafer, the semiconductor device comprising a MOSFET with a pad, the probe card comprising:

a plurality of needles comprising tips positioned to contact the pad, the plurality of needles comprising a plurality of force needles and at least one sense needle; wherein the plurality of force needles are positioned with tips that are equi-distant from a nearest tip of a sense needle of the at least

one sense needle, wherein

the wafer is held by a chuck, and wherein

the probe card is part of a test system comprising the chuck, the testing system configured to provide a current between the plurality of force needles and the chuck along a current path through the chuck, the semiconductor device, the pad, and tips of the plurality of force needles that are in contact with the pad, in such order.

15. The probe card of claim 14, wherein:

the tips of the plurality of force needles are positioned along an arc of a circle around a tip of one sense needle.

16. The probe card of claim 15, wherein:

the at least one sense needle comprises a plurality of sense needles; and a tip of each of the plurality of sense needles is positioned adjacent a tip of the plurality of force needles.

17. A test system for testing a semiconductor device on a wafer, the semiconductor device comprising a pad, the test system comprising:

a chuck positioned to receive the wafer;

a probe card comprising:

a plurality of needles comprising tips positioned to contact the pad, the plurality of needles comprising a plurality of first needles and at least one second needle; wherein the plurality of first needles are positioned with tips that are equi-distant from a nearest tip of a needle of the at least one second needle;

at least one current source coupled to the plurality of first needles and the chuck, the at least one current source configured to induce a current along a current path through the chuck, the semiconductor device, the pad, and tips of the plurality of first needles that are in contact with the pad, in such order; and

at least one voltage sense circuit coupled to the at least one second needle.

18. The test system of claim 17, further comprising:

a processor coupled to receive a value indicative of voltage sensed by the at least one voltage sense circuit and to compute, based on the voltage sensed, an ON resistance of the semiconductor device, wherein the voltage is sensed between the pad and the chuck.

19. The test system of claim 17, wherein the chuck comprises a surface for receiving the wafer and the surface comprises gold plating.

20. The test system of claim 17, wherein the at least one current source is configured to generate a current in excess of 10 Amps.

21. The test system of claim 17, wherein:

the first plurality of needles comprise force needles and the at least one second needle comprises a sense needle.

22. The test system of claim 17, wherein:

the at least one second needle comprises a plurality of second needles; and the plurality of second needles are connected to a single voltage sense circuit of the at least one voltage sense circuit.

23. The test system of claim 22, wherein:

the plurality of second needles are connected to the single voltage sense circuit through equal-valued resistors.

24. The test system of claim 17, wherein:

the chuck comprises a surface for receiving the wafer, and wherein at least a portion of the surface is exposed from the wafer.

25. The test system of claim 17, wherein:

the chuck comprises a surface for receiving the wafer, and wherein the surface is a conductive surface.