INTEGRATED CORE MICROELECTRONIC PACKAGE

BACKGROUND OF THE INVENTION

Field of the Invention: The present invention relates to apparatus and processes for packaging microelectronic dice. In particular, the present invention relates to a packaging technology that encapsulates a microelectronic die within a microelectronic package core.

State of the Art: Higher performance, lower cost, increased miniaturization of integrated circuit components, and greater packaging density of integrated circuits are ongoing goals of the computer industry. As these goals are achieved, microelectronic dice become smaller. Of course, the goal of greater packaging density requires that the entire microelectronic die package be equal to or only slightly larger (about 10% to 30%) than the size of the microelectronic die itself. Such microelectronic die packaging is called a "chip scale packaging" or "CSP".

As shown in FIG. 20, true CSP involves fabricating build-up layers directly on an active surface 204 of a microelectronic die 202. The build-up layers may include a dielectric layer 206 disposed on the active surface 204. Conductive traces 208 may be formed on the dielectric layer 206, wherein a portion of each conductive trace 208 contacts at least one contact 212 on the active surface 204. External contacts, such as solder balls or conductive pins for contact with an external component (not shown), may be fabricated to electrically contact at least one conductive trace 208. FIG. 20 illustrates the external contacts as solder balls 214 which are surrounded by a solder mask material 216 on the dielectric layer 206. However in such true CSP, the surface area provided by the microelectronic die active surface 204 generally does not provide enough surface for

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all of the external contacts needed to contact the external component (not shown) for certain types of microelectronic dice (e.g., logic).

Additional surface area can be provided with the use of an interposer, such as a substrate (substantially rigid material) or a flex component (substantially flexible material). FIG. 21 illustrates a substrate interposer 222 having a microelectronic die 224 attached to and in electrical contact with a first surface 226 of the substrate interposer 222 through small solder balls 228. The small solder balls 228 extend between contacts 232 on the microelectronic die 224 and conductive traces 234 on the substrate interposer first surface 226. The conductive traces 234 are in discrete electrical contact with bond pads 236 on a second surface 238 of the substrate interposer 222 through vias 242 that extend through the substrate interposer 222. External contacts 244 are formed on the bond pads 236 (shown as solder balls). The external contacts 244 are utilized to achieve electrical communication between the microelectronic die 224 and an external electrical system (not shown).

The use of the substrate interposer 222 requires number of processing steps, which increases the cost of the package. Additionally, the use of the small solder balls 228 presents crowding problems which can result in shorting between the small solder balls 228 and can present difficulties in inserting underfill material between the microelectronic die 224 and the substrate interposer 222 to prevent contamination and to increase mechanical reliability. Furthermore, necessity of having two sets of solder balls (i.e., small solder balls 228 and external contacts 244) to achieve connection between the microelectronic die 224 and the external electrical system decreases the overall performance of the microelectronic die package.

Therefore, it would be advantageous to develop new apparatus and techniques to provide additional surface area to form traces for use in CSP applications and eliminate the necessity of the substrate interposer.

BRIEF DESCRIPTION OF THE DRAWINGS

While the specification concludes with claims particularly pointing out and distinctly claiming that which is regarded as the present invention, the advantages of this invention can be more readily ascertained from the following description of the invention when read in conjunction with the accompanying drawings in which:

FIG. 1 is an oblique view of a microelectronic package core, according to the present invention;

FIG. 2 is a top plan via of a microelectronic package core having examples of alternate microelectronic package core openings, according to the present invention;

FIG. 3 is a side cross-sectional view of a microelectronic package core abutted to a protective film, according to the present invention;

FIG. 4 is a side cross-sectional view of microelectronic dice disposed within openings of the microelectronic package core, which also abut the protective film, according to the present invention;

FIG. 5 is a side cross-sectional view of the assembly of FIG. 4 after encapsulation, according to the present invention;

FIG. 6 is a side cross-sectional view of the assembly having microelectronic dice which are thicker than the microelectronic package core after encapsulation, according to the present invention;

FIG. 7 is a side cross-sectional view of the assembly of FIG. 5 after the protective film has been removed, according to the present invention;

FIG. 8 is a side cross-sectional view of an alternate microelectronic package core within a microelectronic assembly, according to the present invention;

FIGs. 9-17 are side cross-sectional views of a process of forming build-up layers on a microelectronic die, encapsulation material, and a microelectronic package core, according to the present invention;

FIG. 18 is a side cross-sectional view of the assembly of FIG. 7 having build-up layers and solder balls positioned thereon, according to the present invention;

FIG. 19 is a side cross-sectional view of a singulated device, according to the present invention;

FIG. 20 is a cross-sectional view of a true CSP of a microelectronic device, as known in the art; and

FIG. 21 is a cross-sectional view of a CSP of a microelectronic device utilizing a substrate interposer, as known in the art.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENT

Although FIGs. 1-19 illustrate various views of the present invention, these figures are not meant to portray microelectronic assemblies in precise detail. Rather, these figures illustrate microelectronic assemblies in a manner to more clearly convey the concepts of the present invention. Additionally, elements common between the figures retain the same numeric designation.

The present invention includes a packaging technology that places at least one microelectronic dice within at least one opening in a microelectronic package core and

secures the microelectronic die/dice within the opening(s) with an encapsulation material. Build-up layers of dielectric materials and conductive traces are then fabricated on the microelectronic die, the encapsulant material, and the microelectronic package core to form a microelectronic package.

The technical advantage of this invention is that the present invention enables the microelectronic package to be built around the microelectronic die. This provides sufficient surface area to position external contacts, while eliminating the need for a substrate interposer, as discussed above. The elimination of the substrate interposer increases the performance of the microelectronic package by eliminating one set of solder connections. Furthermore, the elimination of the substrate interposer increases power delivery performance by bringing the circuitry within the microelectronic die closer to power delivery components (such as decoupling capacitors and the like) of the external electrical system to which the microelectronic package is attached.

FIG. 1 illustrates a microelectronic package core 102 used to fabricate a microelectronic package. The microelectronic package core 102 preferably comprises a substantially planar material. The material used to fabricate the microelectronic package core 102 may include, but is not limited to, a Bismaleimide Triazine ("BT") resin based material, an FR4 material (a flame retarding glass/epoxy material), various polyimide materials, ceramic material, and the like, and metallic materials (such as copper) and the like. The microelectronic package core 102 has at least one opening 104 extending therethrough from a first surface 106 of the microelectronic package core 102 to an opposing second surface 108 of the microelectronic package core 102. As shown in FIG. 2, the opening(s) 104 may be of any shape and size including, but not limited to, rectangular/square 104a, rectangular/square with rounded corners 104b, and circular

104c. The only limitation on the size and shape of the opening(s) 104 is that they must be appropriately sized and shaped to house a corresponding microelectronic die therein, as will be discussed below.

FIG. 3 illustrates the microelectronic package core first surface 106 abutting a protective film 112. The protective film 112 is preferably a substantially flexible material, such as Kapton® polyimide film (E. I. du Pont de Nemours and Company, Wilmington, Delaware), but may be made of any appropriate material, including metallic films. FIG. 4 illustrates microelectronic dice 114, each having an active surface 116 and a back surface 118, placed in corresponding openings 104 of the microelectronic package core 102. In a preferred embodiment (illustrated), the thickness 117 of the microelectronic package core 102 and the thickness 115 of the microelectronic dice 114 are substantially equal. The microelectronic dice 114 are each placed such that their active surfaces 116 abut the protective film 112. The protective film 112 may have an adhesive, such as silicone, which attaches to the microelectronic package core first surface 106 and the microelectronic die active surface 116. This adhesive-type film may be applied prior to placing the microelectronic die 114 and microelectronic package core 102 in a mold or other piece of equipment used for the encapsulation process. The protective film 112 may also be a non-adhesive film, such as a ETFE (ethylene - tetrafluoroethylene) or Teflon® film, which is held on the microelectronic die active surface 116 and the microelectronic package core first surface 106 by an inner surface of the mold or other piece of equipment during the encapsulation process.

The microelectronic die 114 is then encapsulated with an encapsulation material 122, such as plastics, resins, epoxies, and the like. As shown in FIG. 5, the

encapsulation material is disposed in portions of the opening(s) 104 not occupied by the microelectronic die 114. In FIG. 6, an alternate embodiment is shown wherein the microelectronic die thickness 115 is greater than the microelectronic package core thickness 117. Thus, the encapsulation material covers the microelectronic package core second surface 108 and portions of the opening(s) 104 not occupied by the microelectronic die 114, as shown in FIG. 6.

The encapsulation of the microelectronic die 114 may be achieved by any known process, including but not limited to transfer and compression molding, and dispensing. The encapsulation material 122 secures the microelectronic die 114 within the microelectronic package core 102 and provides mechanical rigidity for the resulting structure and provides surface area for the subsequent build-up of trace layers.

After encapsulation, the protective film 112 is removed, as shown in FIG. 7, to expose the microelectronic die active surface 116. As also shown in FIG. 7, the encapsulation material 122 is preferably molded to be a filler for the space between the microelectronic package core first surface 106 and the microelectronic die active surface 116. This results in at least one surface 124 that is substantially planar to the microelectronic die active surface 116 and the microelectronic package core first surface 106. The encapsulation material surface 124 may be utilized in further fabrication steps, along with the microelectronic package core first surface 106, as additional surface area for the formation of build-up layers, such as dielectric material layers and conductive traces.

As shown in FIG. 8, the microelectronic package core 102 may include a plurality of vias 126 extending therethrough and/or a plurality of undercuts or channels 128 in microelectronic package core first surface 106. The embodiment shown in FIG. 8 shows

the microelectronic die thickness 115 greater than the microelectronic package core thickness 117, such as shown in FIG. 6, but is not so limited. Such structures may be used to allow the encapsulation material 122 to flow therein, which will result in a more secure adherence of the encapsulation material 122 to the microelectronic package core 102.

In reference to FIGs. 7 and 8, it is noted that the encapsulation material 122 does not cover the microelectronic die back surface 118. The uncovered microelectronic back surface 118 allows for a heat sink to be directly attached thereto after each microelectronic die 114 has been singulated, as will be discussed below.

Although the following description relates to a bumpless, built-up layer technique for the formation of build-up layers, the method of fabrication is not so limited. The build-up layers may be fabricated by a variety of techniques known in the art.

FIG. 9 illustrates a view of a single microelectronic die 114 encapsulated with encapsulation material 122 within the microelectronic package core 102. The microelectronic die 114, of course, includes a plurality of electrical contacts 132 located on the microelectronic die active surface 116. The electrical contacts 132 are electrically connected to circuitry (not shown) within the microelectronic die 114. Only four electrical contacts 132 are shown for sake of simplicity and clarity.

As shown in FIG. 10, a first dielectric layer 136, such as epoxy resin, polyimide, bisbenzocyclobutene, and the like, is disposed over the microelectronic die active surface 116 (including the electrical contacts 132), the microelectronic package core first surface 106, and the encapsulant material surface 124. The dielectric layers of the present invention are preferably filled epoxy resins available from Ibiden U.S.A. Corp., Santa Clara, California, U.S.A. and from Ajinomoto U.S.A., Inc., Paramus, New Jersey,

U.S.A. The formation of the first dielectric layer 136 may be achieved by any known process, including but not limited to lamination, spin coating, roll coating, and spray-on deposition.

As shown in FIG. 11, a plurality of vias 138 are then formed through the first dielectric layer 136. The plurality of vias 138 may be formed by any method known in the art, including but not limited to laser drilling, photolithography, and, if the first dielectric layer 136 is photoactive, forming the plurality of vias 138 in the same manner that a photoresist mask is made in a photolithographic process, as known in the art.

A plurality of conductive traces 142 is formed on the first dielectric layer 136, as shown in FIG. 12, wherein a portion of each of the plurality of conductive traces 142 extends into at least one of said plurality of vias 138 (see FIG. 11) to make electrical contact with the contacts 108. The plurality of conductive traces 142 may be made of any applicable conductive material, such as copper, aluminum, and alloys thereof.

The plurality of conductive traces 142 may be formed by any known technique, including but not limited to semi-additive plating and photolithographic techniques. An exemplary semi-additive plating technique can involve depositing a seed layer, such as a sputter-deposited or electroless-deposited metal on the first dielectric layer 136. A resist layer is then patterned on the seed layer, such as a titanium/copper alloy, followed by electrolytic plating of a layer of metal, such a copper, on the seed layer exposed by open areas in the patterned resist layer. The patterned resist layer is stripped and portions of the seed layer not having the layer of metal plated thereon is etched away. Other methods of forming the plurality of conductive traces 142 will be apparent to those skilled in the art.

As shown in FIG. 13, a second dielectric layer 144 is disposed over the plurality of conductive traces 142 and the first dielectric layer 136. The formation of the second dielectric layer 144 may be achieved by any known process, including but not limited to film lamination, spin coating, roll coating, and spray-on deposition.

As shown in FIG. 14, a plurality of second vias 146 are then formed through the second dielectric layer 144. The plurality of second vias 146 may be formed any method known in the art, including but not limited to laser drilling and, if the second dielectric layer 144 is photoactive, forming the plurality of second vias 146 in the same manner that a photoresist mask is made in a photolithographic process, as known in the art.

If the plurality of conductive traces 142 is not capable of placing the plurality of second vias 146 in an appropriate position, then other portions of the conductive traces are formed in the plurality of second vias 146 and on the second dielectric layer 144, another dielectric layer formed thereon, and another plurality of vias is formed in the dielectric layer, such as described in FIGs. 12–14. The layering of dielectric layers and the formation of conductive traces can be repeated until the vias are in an appropriate position. Thus, portions of a single conductive trace be formed from multiple portions thereof and can reside on different dielectric layers.

A second plurality of conductive traces 148 may be formed, wherein a portion of each of the second plurality of conductive traces 148 extends into at least one of said plurality of second vias 146. The second plurality of conductive traces 148 each include a landing pad 150 (an enlarged area on the traces demarcated by a dashed line 152), as shown in FIG. 15.

Once the second plurality of conductive traces 148 and landing pads 150 are formed, they can be used in the formation of conductive interconnects, such as solder

bumps, solder balls, pins, and the like, for communication with external components (not shown). For example, a solder mask material 156 can be disposed over the second dielectric layer 144 and the second plurality of conductive traces 154 and landing pads 150. A plurality of vias 160 is then formed in the solder mask material 156 to expose at least a portion of each of the landing pads 150, as shown in FIG. 16. A plurality of conductive bumps 158, such as solder bumps, can be formed, such as by, but not limited to, screen printing solder paste followed by a reflow process or by known plating techniques, on the exposed portion of each of the landing pads 154, as shown in FIG 17.

FIG. 18 illustrates a plurality of microelectronic dice 114 encapsulated with encapsulation material 122 within the microelectronic package core 102. At least one build-up layer is formed on the microelectronic dice active surfaces 116, the microelectronic package core first surface 106, and the encapsulant material surface 124 in the manner previously discussed. The layer(s) of dielectric material and conductive traces comprising the build-up layer is simply designated together as build-up layer 162 in FIG. 18. The individual microelectronic dice 114 are then singulated along lines 164 (cut) through the build-up layer 162 and the microelectronic package core 102 to form at least one singulated microelectronic die package 166, as shown in FIG. 19.

Having thus described in detail embodiments of the present invention, it is understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description, as many apparent variations thereof are possible without departing from the spirit or scope thereof.

CLAIMS

What is claimed is:

1. A microelectronic package, comprising:

a microelectronic package core having a first surface and an opposing second surface, said microelectronic package core having at least one opening defined therein extending from said microelectronic package core first surface to said microelectronic package core second surface;

at least one microelectronic die disposed within said at least one opening, said at least one microelectronic die having an active surface; and

an encapsulation material adhering said microelectronic package core to said at least one microelectronic die.

2. The microelectronic package of claim 1, wherein said encapsulation material further includes at least one surface substantially planar to said microelectronic die active surface and said microelectronic package core first surface.

3. The microelectronic package of claim 2, further including build-up layers disposed on at least one of said microelectronic die active surface, said at least one encapsulation material surface, and said microelectronic package core first surface.

4. The microelectronic package of claim 3, wherein said build-up layers comprise at least one dielectric layer abutting at least one of said microelectronic die active surface, said at least one encapsulation material surface, and said microelectronic

package core first surface and at least one conductive trace disposed on said at least one dielectric layer.

5. The microelectronic package of claim 4, wherein said at least one conductive trace extends through said at least one dielectric layer to contact at least one electrical contact on said microelectronic die active surface.

6. The microelectronic package of claim 1, wherein at thickness of said microelectronic die is greater than a thickness of said microelectronic package core.

7. The microelectronic package of claim 6, wherein said microelectronic package core includes at least one via extending therethrough.

8. The microelectronic package of claim 1, wherein said microelectronic package core is selected from the group consisting of bismaleimide triazine resin based material, an FR4 material, polyimides, ceramics, and metals.

9. A method of fabricating a microelectronic package, comprising:

providing a microelectronic package core having a first surface and an opposing second surface, said microelectronic package core having at least one opening defined therein extending from said microelectronic package core first surface to said microelectronic package core second surface;

disposing at least one microelectronic die within said at least one opening, said at least one microelectronic die having an active surface; and

adhering said microelectronic package core to said at least one microelectronic die with an encapsulation material.

10. The method of claim 9, wherein adhering said microelectronic package core to said at least one microelectronic with said encapsulation material further includes forming at least one encapsulation material surface substantially planar to said microelectronic die active surface and said microelectronic package core first surface.

11. The method of claim 10, further including:

forming at least one dielectric material layer on at least a portion of said microelectronic die active surface, said at least one encapsulation material surface, and said microelectronic package core first surface;

forming at least one via through said at least one dielectric material layer to expose a portion of said microelectronic die active surface; and

forming at least one conductive trace on said at least one dielectric material layer which extends into said at least one via to electrically contact said microelectronic die active surface.

12. The method of claim 11, further including forming at least one additional dielectric material layer disposed over said at least one conductive trace and said at least one dielectric material layer.

13. The method of claim 12, further including forming at least one additional conductive trace to extend through and reside on said at least one additional dielectric material layer.

14. The method of claim 9, wherein said providing said microelectronic package core comprises providing a microelectronic package core selected from the group consisting of bismaleimide triazine resin based material, an FR4 material, polyimides, ceramics, and metals.

15. A method of fabricating a microelectronic package, comprising:

providing a microelectronic package core having a first surface and an opposing second surface, said microelectronic package core having at least one opening defined therein extending from said microelectronic package core first surface to said microelectronic package core second surface;

abutting a protective film against said microelectronic package core first surface, wherein said protective film spans said at least one opening;

disposing at least one microelectronic die within said at least one opening, wherein an active surface of said microelectronic die abuts a portion of said protective film;

adhering said microelectronic package core to said at least one microelectronic die with an encapsulation material, wherein a portion of said encapsulation material fills a portion of said opening to form at least one encapsulation material surface abutting said protective film; and

removing said protective film.

16. The method of claim 15, further including:

forming at least one dielectric material layer on at least a portion of said microelectronic die active surface, said at least one encapsulation material surface, and said microelectronic package core first surface;

forming at least one via through said at least one dielectric material layer to expose a portion of said microelectronic die active surface; and

forming at least one conductive trace on said at least one dielectric material layer which extends into said at least one via to electrically contact said microelectronic die active surface.

17. The method of claim 16, further including forming at least one additional dielectric material layer disposed over said at least on conductive trace and said at least one dielectric material layer.

18. The method of claim 17, further including forming at least one additional conductive trace to extend through and reside on said at least one additional dielectric material layer.

19. The method of claim 15, wherein said providing said microelectronic package core comprises providing a microelectronic package core selected from the group consisting of bismaleimide triazine resin based material, an FR4 material, polyimides, ceramics, and metals.

20. The method of claim 15, wherein said abutting said protective film includes abutting said protective film having an adhesive against said microelectronic package core first surface.

21. A method of fabricating a microelectronic package, comprising:

providing a microelectronic package core having a first surface and an opposing second surface, said microelectronic package core having a plurality of openings defined therein extending from said microelectronic package core first surface to said microelectronic package core second surface;

abutting a protective film against said microelectronic package core first surface, wherein said protective film spans said at least one opening;

disposing a plurality of microelectronic dice within corresponding openings of the microelectronic package core, wherein active surfaces of each of said microelectronic dice abuts a portion of said protective film;

adhering said microelectronic package core to said plurality of microelectronic dice with an encapsulation material, wherein a portion of said encapsulation material fills a portion of said openings to form a plurality of encapsulation material surfaces abutting said protective film;

removing said protective film; and

singulating each microelectronic die by cutting through said microelectronic package core.

22. The method of claim 21, further including:

forming build-up layers on at least a portion of said microelectronic dice active surfaces, said plurality of encapsulation material surfaces, and said microelectronic package core first surface.

23. The method of claim 21, wherein said providing said microelectronic package core comprises providing a microelectronic package core selected from the group consisting of bismaleimide triazine resin based material, an FR4 material, polyimides, ceramics, and metals.

24. The method of claim 21, wherein abutting said protective film includes abutting said protective film having an adhesive against said microelectronic package core first surface.