IMPROVED ETCH STOP LAYER

TECHNICAL FIELD

[0001] The present invention relates generally to semiconductor devices and methods for manufacturing semiconductor devices. In one aspect, the present invention relates to improved methods of forming etch stop layers.

BACKGROUND

[0002] A nitrogen-free etch stop layer is currently preferred for copper dual damascene structures having a low-k dielectric intermetal layer to avoid problems caused by outgassing from the low-k dielectric (e.g., via poisoning, resist scumming, via blinding). Currently a bi-layer structure is often used for providing a nitrogen-free etch stop layer for 90 nm and above technologies, for example. A SiOC layer is currently used as a nitrogen-free etch stop for the dual damascene process. SiOC is currently adopted for its low-k dielectric properties and inter-metal dielectric etch selectivity. A bottom SiC layer is currently used as a glue layer to improve the adhesion between the underlying layer and the etch stop layer. When part of the underlying layer includes copper (e.g., for metal interconnects and/or contacts), the SiC layer also prevents the SiOC from oxidizing the copper. However, a bi-layer structure often causes additional interface adhesion concerns, due in part to the current quality of the SiOC and SiC layers. Also, the use of and processing of the SiOC as the etch stop layer introduces the problem of oxidizing copper in the underlying layer. Thus, it would be desirable to be able to eliminate the bi-layer structure for nitrogen-free etch stop layers, as well as limiting or eliminating the use of SiOC as an etch stop layer material in some cases (e.g., 65 nm technology).

SUMMARY OF THE INVENTION

[0003] The problems and needs outlined above are addressed by embodiments of the present invention. In accordance with one aspect of the present invention, a method of manufacturing a semiconductor device is provided. This method includes the following steps (the order of which may vary). A layer of silicon carbide (SiC) is formed directly on an underlying layer. A dielectric layer is formed directly on the SiC layer. The dielectric layer having a top surface. The dielectric layer is etched to form an opening therein with a first etch chemistry, and the SiC

layer acts as an etch stop layer. A conducting material is deposited into the opening and on the top surface of the dielectric. A portion of the conducting material is removed so that a top surface of the conducting material is substantially planar with the top surface of the dielectric layer. The SiC layer may be etched at the opening with a second etch chemistry. The first etch chemistry is preferably selective against etching SiC. The SiC layer preferably has a thickness between about 20 angstroms and about 550 angstroms. The forming of the SiC layer is preferably performed by flowing substantially pure trimetholsilane (3MS) into a reaction chamber having a pressure of less than about 2 torr therein.

[0004] In accordance with another aspect of the present invention, a semiconductor device is provided. This semiconductor device has a first silicon carbide (SiC) layer formed directly on an underlying layer. It also has a first dielectric layer formed directly on the SiC layer. The first dielectric layer has a top surface. A first conductor extends through the first dielectric layer and the first SiC layer. The first conductor has a top surface. The top surface of the first conductor is substantially planar with the top surface of the dielectric layer. The SiC layer preferably acts as a glue layer and as an etch stop layer.

[0005] In accordance with yet another aspect of the present invention, a semiconductor device is provided. This semiconductor device has a plurality of transistors, each of the transistors having a channel length of 130 nm or less. An oxide layer overlies the plurality of transistors. A silicon carbide (SiC) layer is formed directly on the oxide layer. The dielectric layer is formed directly on the SiC layer. The dielectric layer has a top surface. A conducting material is disposed within a trench formed in the dielectric layer. The conducting material has a top surface. The top surface of the conducting material is substantially planar with the top surface of the dielectric layer. A contact extends through the dielectric layer and the SiC layer to connect one of the transistors to the conducting material. The transistors may be CMOS transistors.

[0006] In accordance with still another aspect of the present invention, a method of manufacturing a semiconductor device is provided. This method includes the following steps (the order of which may vary). A silicon carbide (SiC) etch stop layer is formed on an underlying layer in a reaction chamber with a process that includes the following parameters

(these may be done simultaneous or in a varied order): a) substantially pure trimetholsilane (3MS) is flowed into and through the reaction chamber, and b) the reaction chamber is pressurized at a pressure less than about 2 torr. Then, a dielectric layer is formed over the SiC layer.

[0007] In accordance with another aspect of the present invention, a semiconductor device is provided. This semiconductor device has a layer of silicon carbide (SiC) material formed on an underlying layer. The material properties of the SiC material are such that the SiC material has a current leakage of less than about 1.0×10^{-6} amps per square centimeter at an electric field of about 2 megavolts per centimeter. A dielectric layer is formed over the SiC layer. A conductor (e.g., conducting line, contact, or both) extends through the dielectric layer and the SiC layer. The current leakage is preferably about 1.5×10^{-8} amps per square centimeter at about 2 megavolts per centimeter, and preferably about 1.0×10^{-9} amps per square centimeter at about 1 megavolts per centimeter.

[0008] In accordance with still another aspect of the present invention, a method of manufacturing a semiconductor device is provided. This method includes the following steps (the order of which may vary). A SiOC etch stop layer is formed over an underlying layer (e.g., a SiC layer in a bi-layer etch stop layer structure) in a reaction chamber with a non-He process that includes the following parameters (these may be done simultaneous or in a varied order): a) flowing trimetholsilane (3MS) into and through the reaction chamber; b) flowing CO2 into and through the reaction chamber; c) pressurizing the reaction chamber at a pressure less than about 2 torr; and d) energizing the reaction chamber with low frequency RF power of at least about 100 watts. A dielectric layer is then formed over the SiOC layer. The underlying layer may be a SiC layer or some other layer. The flow rate of the 3MS flowing is preferably about 100 sccm. The flow rate of the CO_2 flowing is preferably about 350 sccm. The process parameters for forming the SiOC layer may further include heating the reaction chamber to a temperature of about 350° C and energizing the reaction chamber with high frequency RF power of at about 400 watts.

[0009] In accordance with yet another aspect of the present invention, a semiconductor device is provided, which includes a layer of silicon carbide (SiC) material, a layer of SiOC material, a dielectric layer, and a conductor. The SiC layer is formed on an underlying layer. The SiOC layer is formed on the SiC layer. The SiOC layer is capable of passing an electron migration test having conditions of about 300° C with a J stress of about 2×10^6 A/cm^2. Also, the SiOC layer is capable of passing a stress migration test having conditions of about 175° C for about 500 hours. The dielectric layer is formed on the SiOC layer. The conductor extends through the dielectric layer, the SiOC layer, and the SiC layer. Also, the SiC material preferably has a current leakage of less than about 1.0×10^{-6} amps per square centimeter at an electric field of about 2 megavolts per centimeter.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0011] Figures 1A and 1B provide simplified cross-section views of a bi-layer nitrogen-free etch stop layer of the prior art;

[0012] Figures 2A-5 provide simplified cross-section views of a single layer nitrogen-free etch stop layer comprising SiC in accordance with a first embodiment of the present invention;

[0013] Figure 6 provides a simplified cross-section view of a second embodiment of the present invention;

[0014] Figure 7 provides a plot comparing a SiC layer formed using the new process with a SiC layer formed using an old process;

[0015] Figures 8-12 provide simplified cross-section views of a third embodiment of the present invention;

[0016] Figures 13-17 provide cross-section views of a fourth embodiment of the present embodiment, as a more specific embodiment;

[0017] Figure 18 provides a simplified cross-section view of a fifth embodiment of the present invention;

[0018] Figure 19 provides a simplified cross-section view of a sixth embodiment of the present invention; and

[0019] Figure 20 provides a simplified cross-section view of a seventh embodiment of the present invention.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0020] The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed herein are merely illustrative of some of the specific ways to make and use the invention, and do not limit the scope of the invention.

[0021] The present invention will be described herein with respect to preferred embodiments in a specific context of semiconductor devices having CMOS technology. The invention may also be applied, however, to other situations.

[0022] Figures 1A and 1B show a contact opening 20 formed with a dual damascene process while using a conventional bi-layer structure 22 for the etch stop layer. As shown in Figure 1B, a current nitrogen-free etch stop layer 22 may have a bulk layer of SiOC 24 formed directly on a thin layer of SiC 26, which is directly formed on the underlying layer 28. The SiOC layer 24 is typically about 530 angstroms thick and the SiC layer 26 is typically about 20 angstroms thick (see Figure 1B), for example.

[0023] A nitrogen-free etch stop layer is currently preferred for copper dual damascene structures having a low-k dielectric intermetal layer to avoid problems caused by outgassing from the low-k dielectric (e.g., via poisoning, resist scumming, via blinding). A SiOC layer 24 in a bi-layer structure 22 is currently used as a nitrogen-free etch stop for the dual damascene process. A SiC layer 26 in a bi-layer structure 22 is sometimes used as a glue layer to improve the adhesion between the underlying layer 28 and the etch stop layer 24. When part of the

underlying layer 28 includes copper (e.g., for metal interconnects and/or contacts), the SiC layer 26 also prevents the SiOC layer 24 from oxidizing the copper (i.e., due to the oxygen contained in the SiOC formation process).

[0024] In a prior bi-layer structure 22 of SiOC 24 and SiC 26, as shown in Figure 1B, the SiC layer 26 is typically lower quality (relative to pure SiC) due to the chemistries used in forming the bi-layer structure 22, which typically consists of a combination of trimetholsilane ($SiH(CH_3)_3$) ("3MS" hereinafter), carbon dioxide (CO_2), and helium (He) (or $3MS/CO_2/He$). Such lower quality SiC has poor electrical properties due to more leakage during time dependent dielectric breakdown (TDDB) tests than the SiOC material used for the etch stop layer 22. However, as described below, the inventors have developed a process for making a higher quality SiC layer (i.e., more pure SiC) with leakage during TDDB tests improved by as much as three orders of magnitude. With this improvement in the resulting SiC layer (due to the developed process), the improved SiC layer can have electrical properties competitive with that of the SiOC material used in the bi-layer etch stop layer structure 22.

[0025] Figures 2A and 2B show an initial structure of a first embodiment 30 of the present invention. In Figure 2A, a SiC layer 32 is formed directly on an underlying layer 28, and a dielectric layer 34 is formed directly on the SiC layer 32. As shown in Figure 2B, the bi-layer structure 22 of Figure 1B may be replaced with a single layer of SiC 32 having a thickness of about 550 angstrom, for example. Hence, the SiC layer 32 acts as both a glue layer for ensuring adhesion between the dielectric layer 34 and the underlying layer 28, and as an etch stop layer used during the formation of a contact opening. Using a single layer of SiC, in accordance with the present invention, may be useful for 65 nm technologies and smaller, for example.

[0026] The dielectric layer 34 is preferably a material having a low dielectric constant (low-k dielectrics) to lower parasitic capacitance and cross-talk between metal lines. The dielectric layer 34 may be composed of any of a variety of dielectric materials, including but not necessarily limited to: silicon dioxide; a diamond-structured carbon (e.g., Black Diamond™ available from Applied Materials); SILK™ available from Dow Chemical; FLARE™ available from Honeywell; LKD (low k dielectric) from JSR Micro; hydrogenated oxidized silicon carbon material (SiOCH) or compounds thereof; amorphous hydrogenated silicon (a-Si:H); silicon-

oxygen-nitrogen compounds (SiOxNy); low-k polymers; organic polymers (e.g., polyimide, parylene, polyarylether, organo-silicone, polynaphthalene, polyquinoline, or copolymers thereof); or combinations thereof, for example. In general, a low-k dielectric can be any dielectric with a dielectric constant lower than that of silicon dioxide.

[0027] The underlying layer 28 may be: another metal layer (e.g., dielectric with conducting material or metal contacts and/or lines formed therein); a substrate having highly doped regions (source, drain); an oxide layer having contacts extending therethrough; and/or a substrate layer having electrical components formed therein (e.g., transistors, capacitors, resistors, diodes, etc.), for example.

[0028] Figures 3-5 illustrate the use of the first embodiment 30 in a dual damascene process for forming an opening. In Figure 3, the dielectric layer 34 has been anisotropically etched using a first photoresist mask (not shown) to form an initial opening 36 in the dielectric layer 34. In Figure 4, the dielectric layer 34 has been anisotropically etched using a second photoresist mask (not shown) to form the remainder of the contact opening 38. The etches performed to achieve the openings 36 and 38 shown in Figures 3 and 4 may be performed using an etch chemistry that is selective against etching SiC, such as a C_5F_8 etch chemistry. Hence, the SiC layer 32 acts as an etch stop layer. In Figure 5, the SiC layer 32 is etched away at the contact opening 38 using another etch chemistry with a good etch selectivity between SiC and low-k dielectric.

[0029] In a second embodiment 40, the SiC layer 32 may be used as an etch stop layer for a single damascene procedure as well, as shown in Figure 6. In a single damascene process, the opening 38 sometimes will not extend all the way through the etch stop layer 32 to the underlying layer 28, such as when the opening 38 is a trench for a conducting line.

[0030] Although not shown in Figures 5 and 6, the damascene process (single or dual), is completed by filling the opening 38 with a conductor, such as copper for example. A copper layer (not shown) typically would be deposited over the device and polished (e.g., chemical-mechanical polishing) back to fill the opening 38. The result is that a top surface of the conducting material will be substantially planar with a top surface 35 of the dielectric layer 34. A specific example of this process is shown in greater detail in Figures 15-17 (discussed below).

[0031] The process of the present invention used to form the higher quality SiC layer 32 that may be used as the etch stop layer while also performing the duty of improving interface adhesion, will be next described. In a preferred process of the present invention, the SiC layer 32 is deposited using a flow of substantially pure 3MS with a flow rate of about 150 sccm, at a temperature of about 350° C, into a reaction chamber (not shown) under a pressure of less than about 2 torr, and submitted to high frequency radio frequency (HFRF) power of about 100 W or more (in AMAT's Producer SE system, for example). The 3MS plasma environment created under these conditions in the reaction chamber induces the formation of the SiC layer 32 on the underlying layer 28. In testing, it has been found that a pressure of about 1.7 torr works well for this process, for example. During the preferred process, the SiC layer 32 is preferably built up to about 550 angstroms, for example, to form a single etch stop layer of SiC, as shown in Figures 2A and 2B. However, the SiC layer 32 may also be built up to another thickness, as needed for a given application. For semiconductor production, the SiC layer 32 may be built up between about 20 angstroms (e.g., in a bi-layer structure as the bottom glue layer) and about 600 angstroms (e.g., a single SiC etch stop layer), for example.

[0032] In contrast, prior used processing methods for forming a bi-layer structure 22 (see e.g., Figure 1B) used 3MS combined with CO_2 and He, which produced the lower quality SiC that is less desirable. The resulting SiC etch stop layer 32 from a preferred process of the present invention has been shown in testing to have an inter-metal dielectric (IMD) TDDB leakage performance improvement (over the prior low quality SiC layer 26 used in the bi-layer structures 22) of about three orders of magnitude when tested at about 2 MV/cm and about 1.5 orders of magnitude performance improvement when tested at about 1 MV/cm. Also, the break down voltage (V_{bd}) at about 1 mA/cm^2 is improved by about three orders of magnitude. A plot from one of such tests is shown in Figure 7, which shows leakage current (in amps per square centimeter) versus electric field (in megavolts per centimeter). In the test used to generate the plot of Figure 7, a 500 angstroms thick layer of SiC was formed using each process (old and new) on a substrate of high-conductivity silicon. The plot in Figure 7 shows the old SiC layer (i.e., formed using a $3MS/CO_2/He$ process as for the bi-layer structure 22) compared with the improved SiC layer (i.e., formed using a process of the present invention; in this case, pure 3MS at about 1.7 torr). Note on the plot in Figure 7 that the current leakage at about 2 megavolts per centimeter is about 1.5×10^{-8} amps per square centimeter for the improved SiC layer formed in

accordance with a preferred embodiment, and the current leakage at about 1 megavolts per centimeter is about 1.0×10^{-9} amps per square centimeter.

[0033] Figures 8-12 show a third embodiment 50 of the present invention to illustrate the use of the present invention during another dual damascene procedure for forming a contact opening 38. In Figure 8, a first SiC etch stop layer 32a is formed directly on an underlying layer 28. A first low-k dielectric layer 34a (e.g., diamond-like carbon) is formed directly on the first SiC etch stop layer 32a. A second SiC etch stop layer 32b is formed directly on the first low-k dielectric layer 34a. A second low-k dielectric layer 34b (e.g., diamond-like carbon) is formed directly on the second SiC etch stop layer 32a. A first opening 36 is etched in the second low-k dielectric layer 34b with an etch chemistry selective against etching SiC (e.g., C_5F_8), as shown in Figure 9. Then, as shown in Figure 10, the second SiC etch stop layer 32b is etched away at the first opening 36 using another etch chemistry that will etch SiC. Next, a second opening 52 is etched in the first low-k dielectric layer 34a with an etch chemistry selective against etching SiC (e.g., C_5F_8), as shown in Figure 11. Then, as shown in Figure 12, the first SiC etch stop layer 32a is etched away at the second opening 52 using another etch chemistry that will etch SiC to complete the contact opening 38.

[0034] In other embodiments (not shown), the first etch stop layer 32a or the second etch stop layer 32b may incorporate a material other than SiC. For example, the SiC material may be more needed for use between the underlying layer 28 and the first dielectric layer 34a (depending on the materials present in the underlying layer 28 and depending on the first dielectric layer material) for purposes of better adhesion among these layers, than for the second etch stop layer between the first and second dielectric layers.

[0035] Figures 13-17 show a fourth embodiment 60 of the present invention, which is a more specific embodiment to illustrate use of the present invention in the production of a semiconductor device. In particular, Figures 13-17 show that the fourth embodiment 60 may be used with a CMOS process that incorporates dual damascene copper metalization with low-k inter-metal insulation, which is a diamond-like carbon material in this example. This embodiment describes just one example, and many other processes for forming other semiconductor devices may also use the present invention.

[0036] Referring first to Figure 13, a semiconductor region 62 is provided, which may include a lightly doped monocrystalline silicon layer. For example, the semiconductor region 62 may include a silicon substrate or a layer upon (e.g., an epitaxial layer or a SOI (silicon-on-insulator) layer) or within (e.g., a well, such as a triple well structure) a silicon substrate.

[0037] Because a CMOS process is being described, two transistors are illustrated. An n-channel MOS transistor 64 is formed in the semiconductor region 62 while a p-channel MOS transistor 66 is formed in an n-well 68. This configuration assumes that the semiconductor region 62 is a lightly doped p-region. If an n-type region is used for the semiconductor region 62, then the n-channel transistor 64 will be formed in the well 68. It is also possible that both transistors 64 and 66 are formed in well regions.

[0038] Aspects of the present invention are useful in small sized semiconductor technologies. For example, an integrated circuit that includes transistors 64 and 66 can be formed using 0.13 μm or 90 nm technology or even smaller (e.g., sub-65 nm technology). In these cases, the transistor channel lengths (of most if not all of the transistors) will be about 0.13μm for the n-channel MOS transistors 64 and about 90 nm or less for the p-channel MOS transistors 66. It is expected that embodiments of the present invention will also be useful at smaller dimensions, e.g., for a physical gate length of 45 nm or less.

[0039] The n-channel transistor 64 is isolated from the p-channel transistor 66 by a shallow trench isolation (STI) region 70. The STI region 70 is formed from a trench about 2500 to about 4000 μm deep in a 6000 μm layer. The trench is filled with an insulator, such as silicon dioxide, for example. Optionally, a more heavily doped semiconductor region 72 may be formed below the STI region 70 to provide further isolation. Alternatively, other isolation, such as field isolation, may be used.

[0040] To form transistor 64 (66), a gate dielectric layer 74/76 and a gate layer 78/80 are formed. As shown in the fourth embodiment, a single gate dielectric layer and a single gate layer are preferably used for both transistors 64 and 66. Either of these layers may be a compound layer. For example, the gate layer 78/80 may include a polysilicon layer and a silicide layer.

[0041] The gate layer 78/80 may be etched to form gates 78 and 80. A lightly doped implant is then formed for each transistor region. Resist may be used to protect the region that is not being doped. Sidewall spacers 82 and 84 are then formed over both gates followed by more heavily doped implants for each transistor. These implants preferably use arsenic and/or phosphorus for the n-channel device and boron for the p-channel device to form the source/drain regions 86 and 88 of the transistors 64 and 66, respectively. Again, resist may be used to protect the region that is not being doped.

[0042] An insulating layer 90 is formed over the device. This insulating layer 90 typically comprises an oxide, such as silicon dioxide, or a doped glass, such as phosphosilicate glass (PSG) or borophosphosilicate glass (BPSG). Vias are formed in the insulating layer 90 and filled with conductive material to form contacts (or plugs) 92. As an example, the conductive material may be tungsten. The two contacts 92 are illustrated as being connected to two arbitrarily chosen regions. It is understood that more (or fewer) contacts could be used and could contact whichever regions the particular design requires.

[0043] Referring now to Figure 14, a SiC etch stop layer 32a is formed over the insulating layer 90 and contacts 92. The SiC etch stop layer 32a may be deposited to a thickness of between about 10 nm (100 angstrom) and about 60 nm (600 angstroms), and preferably about 55 nm (550 angstroms), for example.

[0044] A low-k dielectric layer 34a (e.g., diamond-structured carbon, such as Black Diamond^{TM}) is deposited over the SiC etch stop layer 32a. The low-k dielectric layer 34a may be deposited to a thickness of between about 200 nm and about 800 nm, preferably about 500 nm, for example.

[0045] Referring now to Figure 15, a contact opening is formed in the dielectric layer 34a using a dual damascene process etching down to the etch stop layer 32a using a first etch chemistry that is selective against etching SiC. The etch stop layer 32a at the contact opening is then etched away using a second etch chemistry that will etch the SiC.

[0046] Referring now to Figure 16, a dual damascene interconnect structure is shown in Figure 16. The illustration of this structure includes two contacts and lines 94a, although it is

understood that other configurations can be used. While a dual damascene process is illustrated, it should be understood that other processes such as single damascene or contact via formation techniques (as shown for contacts 92) may be used.

[0047] In the dual damascene process, trenches are formed within the dielectric layer 34a and contact holes are formed within the trenches to contact selected portions beneath the dielectric layer 34a. The trenches and contact vias can then be filled with a conducting material, preferably copper. Typically, the conducting material (e.g., 94a) is deposited into the openings 38 and onto a top surface (e.g., 35a) of the dielectric layer (e.g., 34a). Then, the conducting material 94a is polished back so that a top surface 95a of the conducting material 94a is substantially planar with the top surface 35a of the dielectric layer 34a, as shown in Figure 17 for example. Further details on dual damascene processes that include low-k dielectric layers can be found in the following patents, each of which is incorporated herein by reference: U.S. Patent No. 6,342,448 entitled "Method of fabricating barrier adhesion to low-k dielectric layers in a copper damascene process;" U.S. Patent No. 6,319,809 entitled "Method to reduce via poison in low-k Cu dual damascene by UV-treatment;" and U.S. Patent No. 6,211,061 entitled "Dual damascene process for carbon-based low-K materials."

[0048] As illustrated in Figure 17, more than one layer of metalization may be included. In this device five levels of metal 94a, 94b, 94c, 94d, and 94e are shown. While the illustrated embodiment shows five layers, it is understood that a semiconductor device of the preferred embodiment could include more (or fewer) than five layers of metalization. For example, a chip might include up to eight layers or more in 0.13 μm technology. Each of these layers may be processed using the steps described herein. In other embodiments (not shown), SiC may be used for only some of the etch stop layers 32a, 32b, 32c, 32d, and 32e, depending on the needs of the design and the materials used.

[0049] Figure 18 shows a fifth embodiment 100 of the present invention to illustrate the use of an improved SiC layer in accordance with the present invention within a bi-layer etch stop layer structure 122. In the fifth embodiment 100, the SiC layer 32 is formed using a preferred process of the present invention (e.g., pure 3MS at about 1.7 torr, as described above in relation to FIG. 7). In the fifth embodiment 100, the SiOC layer 24 is formed using prior methods.

[0050] Figure 19 shows a sixth embodiment 110 of the present invention to illustrate the use of an improved SiOC layer 124 and an improved SiC layer 32 in accordance with the present invention within a bi-layer etch stop layer structure 122. As in the fifth embodiment 100, the SiC layer 32 of the six embodiment 110 is formed using a preferred process of the present invention (e.g., pure 3MS at about 1.7 torr, as described above in relation to FIG. 7).

[0051] In the past, the SiOC layer was often formed using a process that included helium. The improved SiOC layer 124 in the sixth embodiment 110 is formed using a preferred process for forming the SiOC layer 124 of the present invention. In this preferred process, the SiOC layer 124 is deposited using a flow of substantially pure 3MS with a flow rate of about 100 sccm and a flow of CO_2 with a flow rate of about 350 sccm, into a reaction chamber (not shown), at a temperature of about 350° C, under a pressure of less than about 2 torr, and submitted to high frequency radio frequency (HFRF) power of about 400 W and a low frequency radio frequency (LFRF) of about 100 W or more (in AMAT's Producer SE system, for example). The 3MS/CO_2 plasma environment created under these conditions in the reaction chamber induces the formation of the improved SiOC layer 124 on the SiC layer 32. This preferred process provides a non-helium (non-He) method of forming an improved SiOC layer 124. In testing, it has been found that a pressure of about 1.7 torr works well for this process, for example. One of the keys to this preferred process of forming an improved SiOC layer 124 is the use of 100 W or more LFRF power. In one use of the preferred process, it has been found that a LFRF of about 200 W works well.

[0052] For example, as compared to prior processes for forming a SiOC layer using a pressure of greater than 2 torr, using a flow of He in combination with a 3MS and CO_2 flow, and/or not using LFRF, the improved SiOC layer formed using the preferred process of the present invention provides improved electron migration (EM) and stress migration (SM) test results. An improved SiOC layer formed using a preferred process (non-He process) of the present invention has passed EM tests having conditions of about 300° C with a J stress of about 2×10^6 A/cm^2 and has passed SM tests having conditions of about 175° C for about 500 hours to see RC shift (with a RC via size of about 0.13 μm). The lower pressure (i.e., less than about 2 torr) also improves film quality in the SiOC layer 124 and the SiC layer 32.

[0053] Figure 20 shows a seventh embodiment 120 of the present invention to illustrate the use of an improved SiOC layer 124 in accordance with the present invention within a bi-layer etch stop layer structure 122. In the seventh embodiment 120, the SiOC layer 124 is formed using a preferred process of the present invention (e.g., a flow of 3MS/CO_2 at less than about 2 torr with a LFRF of about 100 W or more, as described above in relation to the sixth embodiment 110). In the seventh embodiment 120, the SiC layer 26 is formed using prior methods.

[0054] Some of the advantages that may be achieved using a process of the present invention and using an embodiment of the present invention are listed below. Various embodiments of the present invention may include some or all of these advantages, and other advantages not listed may also exist:

[0055] 1. Improving electrical properties for the SiC layer with respect to TDDB tests;

[0056] 2. Ability to have a single-layer nitrogen-free etch stop layer that performs at least as well as a nitrogen-free etch stop layer having a bi-layer structure of SiOC and SiC;

[0057] 3. Ability to have a simpler process with less steps for forming an etch stop layer (for single SiC layer etch stop layer), as compared to bi-layer structure;

[0058] 4. Ability to have dual functions of the SiC layer acting as an etch stop layer and as a glue layer

[0059] 5. Improving interface adhesion (for single SiC layer etch stop layer), as compared to bi-layer structure;

[0060] 6. Ability to provide a low-dielectric-constant etch stop layer to improve RC delay;

[0061] 7. Providing less or no concern of the etch stop layer oxidizing copper that may be present in the underlying layer (such oxidation would likely cause worse RC delay) (for single SiC layer etch stop layer);

[0062] 8. Providing higher etch selectivity of SiC with respect to the dielectric layer (e.g., Black Diamond® material) (for single SiC layer etch stop layer as compared to SiOC) due to a higher carbon difference;

[0063] 9. Providing better etch selectivity than a SiOC etch stop layer with respect to low-k SiOC (for single SiC layer etch stop layer), which is sometimes used as the dielectric layer;

[0064] 10. Avoiding an additional layer interface to eliminate possible additional adhesion concerns (for single SiC layer etch stop layer as compared to bi-layer structure);

[0065] 11. Outstanding moisture resistance (for single SiC layer etch stop layer);

[0066] 12. Improved film quality for SiC layer and/or SiOC layer;

[0067] 13. Improved performance in EM and SM tests for SiOC layer;

[0068] 14. Providing a non-He method of forming SiOC layer; and

[0069] 15. Improving reliability of a device incorporating an improved SiOC layer and/or SiC layer in accordance with the present invention.

[0070] Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the processes, materials, and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, materials, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

CLAIMS:

1. A method of manufacturing a semiconductor device, comprising:

forming a silicon carbide (SiC) etch stop layer on an underlying layer in a reaction chamber with a process comprising:

flowing substantially pure trimetholsilane (3MS) into and through the reaction chamber, and

pressurizing the reaction chamber at a pressure less than about 2 torr; and

forming a dielectric layer over the SiC layer.

2. The method of claim 1, wherein the flow rate of the 3MS flowing is about 150 sccm, and wherein the process of forming the SiC layer further comprises:

energizing the reaction chamber with high frequency RF power of at least about 100 watts; and

heating the reaction chamber to a temperature of about 350°C.

3. A method of manufacturing a semiconductor device, comprising:

forming a layer of silicon carbide (SiC) directly on an underlying layer, wherein forming of the SiC layer comprises flowing substantially pure trimetholsilane (3MS) into a reaction chamber having a pressure of less than about 2 torr therein;

forming a dielectric layer directly on the SiC layer, the dielectric layer having a top surface;

etching the dielectric layer to form an opening therein with a first etch chemistry, wherein the SiC layer acts as an etch stop layer and etching the SiC layer at the opening with a second etch chemistry;

depositing a conducting material into the opening and on the top surface of the dielectric; and

removing a portion of the conducting material so that a top surface of the conducting material is substantially planar with the top surface of the dielectric layer.

4. The method of claim 3, wherein the etching of the dielectric layer includes a dual damascene process for forming the opening.

5. The method of claim 3 or 4, wherein the first etch chemistry is selective against etching SiC.

6. The method of any one of claims 3-5, wherein the removing of the conducting material portion is by polishing.

7. The method of any one of the preceding claims, wherein SiC layer has a thickness between about 20 angstroms and about 550 angstroms, wherein the underlying layer is an oxide layer formed over a plurality of CMOS transistors, and wherein the dielectric layer is composed of a dielectric material including a diamond-structured carbon material.

8. The method of any one of claims 3-7, wherein the flowing of the 3MS occurs at a flow rate of about 150 sccm, wherein the reaction chamber has a temperature of about 350°C therein, and wherein high frequency RF power of at least about 100 watts is applied in the reaction chamber to induce the formation of the SiC layer on the underlying layer.

9. The method of claim 8, wherein the pressure within the reaction chamber is about 1.7 torr.

10. A semiconductor device manufactured according to any one of method claims 1-9.

11. The device of claim 10, wherein the SiC layer has a thickness of about 550 angstroms.

12. The device of claim 10 or 11, wherein the SiC layer acts as a glue layer and as an

etch stop layer.

13. The device of any one of claims 10-12, wherein the conducting material includes copper.

14. The device of any one of claims 10-13, wherein the dielectric layer is composed of a dielectric material including a diamond-structured carbon material.

15. The device of any one of claims 10-13, wherein the dielectric layer is composed of a dielectric material including a SiOCH material.

16. The device of any one of claims 10-13, wherein the dielectric layer is composed of SiOC.

17. The device of any one of claims 10-16, wherein the underlying layer is an oxide layer.

18. The device of claim 17, further comprising a plurality of CMOS transistors being covered by the oxide layer.

19. The device of any one of claims 10-18, further comprising:

a second silicon carbide (SiC) layer formed directly on the (first) dielectric layer;

a second dielectric layer formed directly on the second SiC layer;

a second conductor extending through the second dielectric layer and the second SiC layer and connecting to the (first) conductor.

20. The device of claim 19, further comprising:

a third silicon carbide (SiC) layer formed directly on the second dielectric layer;

a third dielectric layer formed directly on the third SiC layer;

a third conductor extending through the third dielectric layer and the third SiC layer and connecting to the second conductor;

a fourth silicon carbide (SiC) layer formed directly on the third dielectric layer;

a fourth dielectric layer formed directly on the fourth SiC layer; and

a fourth conductor extending through the fourth dielectric layer and the fourth SiC layer and connecting to the third conductor.

21. The device of claim 20, wherein each of the first, second, third, and fourth conductors are composed of a conducting material that includes copper, and wherein each of the first, second, third, and fourth dielectric layers is composed of a low-k dielectric material selected from a group consisting of SiCOH and diamond-structured carbon.

22. A semiconductor device comprising:

a plurality of transistors, each of the transistors having a channel length of 130 nm or less;

an oxide layer overlying the plurality of transistors;

a silicon carbide (SiC) layer formed directly on the oxide layer;

a dielectric layer formed directly on the SiC layer, the dielectric layer having a top surface;

a conducting material disposed within a trench formed in the dielectric layer, the conducting material having a top surface, wherein the top surface of the conducting material is substantially planar with the top surface of the dielectric layer; and

a contact extending through the dielectric layer and the SiC layer to connect one of the transistors to the conducting material;

wherein the silicon carbide layer is formed according to any one of the method claims 1-9.

23. The device of claim 22, wherein the transistors are CMOS transistors.

24. The device of claim 22 or 23, wherein the SiC layer has a thickness between about 20 angstroms and about 600 angstroms.

25. A semiconductor device comprising:

a layer of silicon carbide (SiC) material formed on an underlying layer, wherein the SiC material is formed according to any one of method claims 1-9 and the SiC material has a current leakage of less than about 1.0×10^{-6} amps per square centimeter at an electric field of about 2 megavolts per centimeter;

a dielectric layer formed over the SiC layer; and

a conductor extending through the dielectric layer and the SiC layer.

26. The semiconductor device of claim 25, wherein the current leakage at about 2 megavolts per centimeter is about 1.5×10^{-8} amps per square centimeter.

27. The semiconductor device of claim 27 or 28, wherein the current leakage at about 1 megavolts per centimeter is about 1.0×10^{-9} amps per square centimeter.

28. A method of manufacturing a semiconductor device, comprising:

forming a SiOC etch stop layer over a SiC underlying layer in a reaction chamber with a process comprising:

flowing substantially pure trimetholsilane (3MS) into and through the reaction chamber,

flowing CO_2 into and through the reaction chamber,

pressurizing the reaction chamber at a pressure less than about 2 torr, and

energizing the reaction chamber with low frequency RF power of at least about 100 watts; and

forming a dielectric layer over the SiOC layer,

wherein the SiC layer is formed by flowing a substantially pure trimetholsilane (3MS) into and through the reaction chamber and pressurizing the reaction chamber at a pressure less than about 2 torr in a step separate from the SiOC forming step.

29. The method of claim 28, wherein the process of forming the SiOC etch stop layer is a non-He process.

30. The method of claim 28 or 29, wherein the flow rate of the 3MS flowing is about 100 sccm.

31. The method of any one of claims 28-30, wherein the flow rate of the CO_2 flowing is about 350 sccm.

32. The method of any one of claims 28-31, wherein the process of forming the SiOC layer further comprises:

heating the reaction chamber to a temperature of about 350°C; and

energizing the reaction chamber with high frequency RF power of at about 400 watts.

33. A semiconductor device manufactured according to any one of method claims 28-32.

34. A semiconductor device comprising:

a layer of silicon carbide (SiC) material formed on an underlying layer according to any one of method claims 1-9;

a layer of SiOC material formed on the SiC layer, wherein the SiOC layer is formed according to any one of method claims 28-32, wherein the SiOC material exceeds both an electron migration test having conditions of about 300°C with a J stress of about 2×10^6 A/cm2 and capable of passing a stress migration test having conditions of about 175°C for about 500 hours;

a dielectric layer formed on the SiOC layer; and

a conductor extending through the dielectric layer, the SiOC layer, and the SiC layer.

35. The semiconductor device of claim 34, wherein the SiC material has a current leakage of less than about 1.0×10^{-6} amps per square centimeter at an electric field of about 2 megavolts per centimeter.