DOUBLE BUMPING OF FLEXIBLE SUBSTRATE FOR FIRST AND SECOND LEVEL INTERCONNECTS

TECHNICAL FIELD

The present invention relates generally to methods and apparatus of preparing and forming interconnections on an interposer substrate for assembling one or more semiconductor dice thereto and, particularly, providing interconnections on the interposer substrate for a first level interconnect and a second level interconnect.

BACKGROUND

State of the Art: Interconnection and packaging-related issues are among the factors that determine not only the number of circuits that can be integrated on a chip but also the performance of the chip. These issues have gained importance as advances in chip design have led to reduced sizes of transistors and enhanced chip complexity. The industry has come to realize that merely having a fast chip will not necessarily result in a fast system; the fast chip must also be supported by equally fast and reliable connections. Essentially, the connections, in conjunction with the packaging, supply the chip with signals and power and redistribute the tightly packed terminals of the chip to the terminals of a carrier substrate and then to a circuit board.

One example of such an integrated circuit device is known as a "flip-chip." Flip-chip attachment generally includes electrically and mechanically attaching a semiconductor die by its active surface to an interposer substrate or other carrier substrate using an array of discrete conductive elements formed on the semiconductor die. The discrete conductive elements are formed and bonded to bond pads on the active surface of the semiconductor die, usually during fabrication of the semiconductor die along with a large number of others in wafer form, after which the wafer is singulated into the individual semiconductor die.

The discrete conductive elements usually are configured as minute conductive bumps or balls, but also may include studs, pillars or columns of various configurations. The conductive bumps or discrete conductive elements are typically, in the case of solder balls, attached to the bond pads by first forming an under bump metal (UBM) compatible with the material of the bond pads, as well as the solder balls.

The UBM for solder balls to be placed on aluminum bond pads commonly includes metal layers, bottom to top, of Cr, Cu and Au. The UBM may be formed by sputtering thin films over the aluminum bond pad through a patterning and etching process. The UBM may also be formed by an electroplating process of Cu and/or Ni with a thin Au overlay. A preformed solder ball (of, for example, 60% Sn and 40% Pb) may then be provided on the UBM and heated to a predetermined reflow temperature so as to bond the solder balls to the UBM structures on the wafer. Alternatively, a solder paste may be disposed on the UBM and then heated to liquify and form a solder ball.

Each discrete conductive element is placed corresponding to mutually aligned locations of bond pads (or other I/O locations) on the semiconductor die and terminals on the carrier substrate when the two components are superimposed. The semiconductor die is thus electrically and mechanically connected to the carrier substrate by, for example, reflowing conductive bumps of solder or curing conductive or conductor-filled epoxy bumps. A dielectric underfill may then be disposed between the die and the carrier substrate for environmental protection and to enhance the mechanical attachment of the die to the carrier substrate. For example, United States Patent No. 5,710,071 to Beddingfield et al. discloses a fairly typical flip-chip attachment of a bumped semiconductor die to a carrier substrate and a method of underfilling a gap between the semiconductor die and substrate.

Flip-chip type assemblies having a bumped semiconductor die employing a carrier substrate, such as the carrier substrate disclosed in the Beddingfield et al. reference, may be undesirably thick due to the combined height of the bumped semiconductor die and carrier substrate. Ongoing goals of the computer industry include higher performance, lower cost, increased miniaturization of components, and greater packaging density of integrated circuits in, for example, a flip-chip type assembly. In an effort to meet goals such as increased miniaturization by limiting the height of a flip-chip type assembly, thin flexible interposer substrates have been introduced in the industry.

U.S. Patent No. 5,386,341 to Olson et al. discloses such a thin flexible substrate utilized as an interposer substrate between a bumped semiconductor die and a circuit board. However, thin flexible substrates, such as that disclosed in the Olson et al. reference, require that bumps formed on the semiconductor dice be formed precisely to

predetermined specifications with very low dimensional tolerances. Any failure in forming the bumps and interconnections on the semiconductor dice precisely so that the semiconductor dice align with corresponding terminals on an interposer substrate typically results in unusable semiconductor dice. Such unusable semiconductor dice may be scrapped, which is extremely costly, as a result of bad interconnections. These reliability issues are only compounded with the increased miniaturization of the semiconductor components. Furthermore, the method of forming the UBM structures and conductive bumps or solder balls on each of the bond pads on the wafer is consumptive of time, process and materials and, thus, costly.

Therefore, it would be advantageous to limit the time required for wafer bumping including the respective formation and attachment of the UBM structure and solder balls on the wafer. It would also be advantageous to prevent the loss of semiconductor dice due to failed interconnections on the semiconductor dice.

DISCLOSURE OF INVENTION

The present invention relates to methods and apparatus for improving the yield and reducing the cost of fabricating a flip-chip type semiconductor assembly. The present invention is directed to forming an interposer substrate with interconnections formed on both a first surface and a second surface to provide a respective first level interconnect and a second level interconnect. The interposer substrate may include first and second sets of conductive bumps respectively formed on the first surface and second surface thereof. Both sets of conductive bumps may be formed simultaneously by an electrolytic or electroless process. The first set of conductive bumps may be configured to correspond with bond pad locations on at least one bumpless semiconductor die for the first level interconnect and the second set of conductive bumps may be configured to correspond with a pattern of interconnections on a circuit board or another semiconductor assembly for the second level interconnect. With this arrangement, the present invention provides structure for effecting interconnections on the interposer substrate for both a first level interconnection and second level interconnection, thereby eliminating the need for wafer bumping and the costs and reliability issues associated therewith. Furthermore, transferring such costs and reliability issues from fabrication of semiconductor dice on a wafer to fabrication of the

far less expensive interposer substrate greatly reduces the cost of any defective parts that must be scrapped.

In one aspect of the present invention, the interposer substrate includes through holes extending between the first surface and the second surface thereof. Conductive lines may be formed over the first surface to extend from the through holes to remote locations on the first surface that correspond with locations of the bond pads of a bare semiconductor die. A plating process may then be conducted to form a first set of conductive bumps at such alternate locations. The plating process may also be used to simultaneously form a second set of conductive bumps in the through holes on the second surface of the interposer substrate for the second level interconnection to, for example, a circuit board. Alternatively, the second set of conductive bumps may also include a conductive paste disposed in the through holes, wherein conductive balls, such as solder balls, may be provided in the conductive paste on the second surface of the interposer substrate.

According to the present invention, the plating process for simultaneously forming the first and second sets of conductive bumps on the respective first surface and second surface may be accomplished chemically in an electroless process or electrochemically in an electrolytic process. The conductive materials that may be utilized in forming the conductive bumps may include at least one of copper, nickel, chromium, zinc, brass, cadmium, silver, tin and gold.

In another aspect of the present invention, a dielectric filler material may be disposed between the at least one bumpless semiconductor die and the interposer substrate. The filler material may be provided by dispensing a flowable dielectric filler material to fill a gap between the bumpless semiconductor die attached to the interposer substrate. Alternatively, the dielectric filler material may be a nonflowable filler material, in which case the nonflowable filler material may comprise a dielectric filler film. The dielectric filler film is adhesively attached to either the semiconductor die or interposer substrate prior to attaching the bumpless semiconductor die to the interposer substrate.

In another aspect of the present invention, the semiconductor device assembly of the present invention is mounted to a circuit board in an electronic system, such as a computer system. In the electronic system, the circuit board is electrically connected to

a processor device, which communicates with an input device and an output device.

Other features and advantages of the present invention will become apparent to those of skill in the art through a consideration of the ensuing description, the accompanying drawings and the appended claims.

BRIEF DESCRIPTION OF DRAWINGS

While the specification concludes with claims particularly pointing out and distinctly claiming that which is regarded as the present invention, the advantages of this invention may be ascertained from the following description of the invention when read in conjunction with the accompanying drawings, wherein:

FIG. 1 illustrates a simplified cross-sectional view of an interposer substrate, depicting the interposer substrate having through holes formed therein, according to the present invention;

FIG. 1A illustrates a simplified cross-sectional view of an interposer substrate, depicting an alternative through hole formed in the interposer substrate, according to the present invention;

FIG. 2 illustrates a simplified cross-sectional view of the interposer substrate, depicting conductive lines formed on the interposer substrate, according to the present invention;

FIG. 3 illustrates a simplified cross-sectional view of the interposer substrate, depicting the interposer substrate having bumps and a protective layer formed thereon, according to the present invention;

FIG. 3A illustrates a simplified cross-sectional view of the interposer substrate, depicting an alternative method of arranging the conductive lines and bumps formed on the interposer substrate, according to the present invention;

FIG. 4 illustrates a simplified cross-sectional view of a bumpless semiconductor die facing the bumped interposer substrate in an unattached position, according to the present invention;

FIG. 5 illustrates a simplified cross-sectional view of the bumpless semiconductor die attached to the interposer substrate with filler material dispensed therebetween, according to the present invention;

FIG. 6 illustrates a cross-sectional view of an alternative method of forming a filler material between a bumpless semiconductor die and an interposer substrate, depicting the bumpless semiconductor die facing the bumped interposer substrate in an unattached position with a nonflowable filler material disposed over the interposer substrate, according to the present invention;

FIG. 7 illustrates a simplified cross-sectional view of the nonflowable filler material alternatively disposed between the bumpless semiconductor die attached to the interposer substrate, according to the present invention;

FIG. 8 illustrates a simplified top view of the interposer substrate having an array of die attach sites, depicting semiconductor dice attached to the die attach sites, according to the present invention;

FIG. 9 illustrates a simplified cross-sectional view of a singulated semiconductor assembly having an encapsulation material formed thereover, according to the present invention;

FIG. 10 illustrates a second embodiment of an interposer substrate depicting multiple levels of conductive lines in the interposer substrate, according to the present invention;

FIG. 11 illustrates a simplified side view of the interposer substrate with multiple levels attached to multiple semiconductor dice, according to the present invention; and

FIG. 12 illustrates a block diagram of the semiconductor assembly of the present invention interconnected to an electronic system, according to the present invention.

BEST MODE(S) FOR CARRYING OUT THE INVENTION

Embodiments of the present invention will be hereinafter described with reference to the accompanying drawings. It would be understood that these illustrations are not to be taken as actual views of any specific apparatus or method of the present invention, but are merely exemplary, idealized representations employed to more clearly and fully depict the present invention than might otherwise be possible. Additionally, elements and features common between the drawing figures retain the same or similar numerical designation.

FIGS. 1-3 illustrate a process that may be used for fabricating an interposer substrate having a first and second level interconnects formed thereon. Referring first to FIG. 1, an interposer substrate 110 including a first surface 112 and a second surface 114 is depicted. Interposer substrate 110 may comprise a flexible material, such as, for example, a polyimide or other polymeric material. Interposer substrate 110 is utilized to provide an electrical interconnect between one or more semiconductor dice and other electronic components located external to interposer substrate 110.

The interposer substrate 110 may include through holes 116 extending between the first surface 112 and second surface 114 thereof for electrically interconnecting a semiconductor chip to external components, as explained hereinafter. The through holes 116 may include tapered, frustoconical walls 118 extending between the first surface 112 and second surface 114, which, as shown, taper inward from the second surface 114 of the interposer substrate 110. The tapered through holes 116 may be formed using any suitable method known in the art, such as, for example, a wet chemical etch or laser ablation.

Through holes 116 formed using a wet etch may result in a tapered wall angle of approximately 0.785 radians from the vertical, which angle may vary depending on the type of reactive chemical etchant utilized for removing the interposer substrate material. From a production standpoint, such wet etching may be preferred since many interposer substrates may be processed at a relatively minimal process time. On the other hand, while laser ablation techniques may be more time consuming, they provide greater versatility in forming a broad range of tapered angles, which may be advantageous depending on the requirements of the designer of the interposer substrate.

Alternatively, as illustrated in FIG. 1A, interposer substrate 110 may include through holes 116 therein formed using a mechanical punch, as known in the art. The punch may be configured to form any shape of through hole, such as circular, square and the like, wherein the through holes 116 are defined by parallel punched walls 119. The punched walls 119 may substantially extend orthogonal to the first surface 112 and the second surface 114 of the interposer substrate 110.

FIG. 2 illustrates the interposer substrate 110 with conductive lines 120 formed on a first surface 112 thereof. Preferably, the conductive lines 120 are a copper or a copper alloy material. However, conductive lines 120 may include any suitable

electrically conductive material such as, for example, gold, aluminum, nickel and alloys thereof.

The conductive lines 120 may be formed by any known method in the art, such as deposition and etching processes, screen printing or a tape carrying preformed conductive traces, etc. By way of example, the conductive lines 120 may be formed by depositing a layer of conductive material over the first surface 112 of the interposer substrate 110. Such depositing of conductive material may be accomplished by physical vapor deposition, chemical vapor deposition, sputtering, screen printing, vacuum deposition, or other any known method of depositing a thin conductive material. The layer of conductive material may then be selectively masked and patterned using a positive or negative photoresist as known in the art followed by etching using a wet or dry etch to form the conductive lines 120.

The conductive lines 120 may extend over the first surface 112 so that a first portion 122 extends over a through hole 116 and a second portion 124 extends to a predetermined position remote from the associated through hole 116 on the first surface 112 of the interposer substrate 110. Such a predetermined remote position is selected to proximately correspond with a first level interconnect pattern, such as a bond pad pattern of a semiconductor die. In this manner, multiple conductive lines 120 may be formed so that each conductive line 120 may extend from and/or over a through hole 116 to a predetermined remote position on the first surface 112 of the interposer substrate 110.

FIG. 3 illustrates the interposer substrate 110 with conductive bumps 130 formed on the first surface 112 and conductive bumps 132 formed on the second surface 114 of the interposer substrate 110. Prior to forming the conductive bumps 130, the conductive lines 120 may have a protective layer 134 applied thereover. The protective layer 134 may comprise any electrical and environmental barrier formed of any known material, such as a solder resist. The protective layer 134 may be provided in the form of an epoxy-based paste or in dry film form, which serves as a surface insulator and mask for those areas where electrical interconnection and plating is not wanted. The protective layer 134 may be blanket deposited and selectively etched to form apertures exposing the second portions 124 of the conductive lines 120. By this arrangement, the second portions 124 of the conductive lines 120 may be exposed for

facilitating the formation of the conductive bumps 130 thereon. It is also contemplated that a protective layer 134 comprising, for example, a solder resist, may be applied over second surface 114. Use of, for example, a dry film protective layer 134 not only protects conductive lines 120 but, as best shown in FIG. 3, precise location of the apertures and sizing and configuration of the apertures formed in a protective layer 134 facilitates formation of conductive bumps 130 and 132 and enables a finer design rule as to bump size and pitch.

The conductive bumps 130 may be formed on the exposed second portion 124 of the conductive lines 120 by an electrolytic plating process or an electroless plating process. Such conductive bumps 130 may be sized and configured in the predetermined locations of the second portion 124 of the conductive lines 120 to correspond with bond pads of a semiconductor die (not shown). Alternatively, the conductive bumps 130 may be formed in recesses 136 so that the conductive bumps 130 abut with an end 126 of the second portion 124 while also being disposed in the recesses 136 (see FIG. 3A). Such a recess for the conductive bumps to be disposed in may result in a reduction of height in the conductive bumps 130 with respect to the interposer substrate 110 compared to providing the conductive bumps 130 directly on the conductive lines 120. In either case, the conductive bumps 130 are configured to slightly protrude from the first surface 112 of the interposer substrate 110 as a first level interconnect and configured to correspond to and interconnect with a bond pad outline on a semiconductor die.

Conductive bumps 132 are formed in the through holes 116 and are sized and configured to protrude slightly from the second surface 114 of the interposer substrate 110. The conductive bumps 132 may be configured to electrically and mechanically interconnect with the first portions 122 of the conductive lines 120 that extend to and/or over the through holes 116 on the first surface 112 of the interposer substrate 110. The conductive elements 132 are configured in an array as a second level interconnect and configured to correspond to and interconnect with a terminal pad pattern of a circuit board, other higher-level packaging or even another semiconductor substrate. It should also be noted that conductive lines 120, as shown in broken lines in FIG. 3A, may be formed on second surface 114 of interposer substrate 110 and contacted by conductive bumps 132. Recesses 136 may be extended, also as shown in broken lines in FIG. 3A,

for contact of conductive bumps 130 formed therein with the conductive lines 120 on second surface 114. Thus it will be apparent that conductive lines 120 may be used on either the first surface 112, the second surface 114, or both as desired or required, in accordance with the present invention.

According to the present invention, both the conductive bumps 130 and the conductive bumps 132 may be formed simultaneously by the above-referenced electrolytic plating or electroless plating processes. As is well known in the art, an electrolytic plating process is a metal deposition process in which an electrolyte, or a solution containing dissolved salts of the metal to be plated, transfers cations from an anode into the electrolyte and onto the exposed first portions 122 and second portions 124 of conductive lines 120 serving as a cathode by means of a direct electrical current applied to the electrolyte from the anode to the cathode. The metal may be caused to deposit and build up to a predetermined size to form the conductive bumps 130 and conductive bumps 132 on the exposed second portions 124 of the conductive lines 120 and the exposed first portions 122 of the conductive lines 120 extending over the through hole 116, respectively, in the interposer substrate 110.

Likewise, the conductive bumps 130 and conductive bumps 132 may be formed simultaneously on the interposer substrate 110 in an electroless plating process. As is well known in the art, an electroless plating process comprises the deposition of metallic particles from a chemical solution, usually at elevated temperatures, without an electrical current flowing as is used in the electrolytic plating process. The electroless plating process is highly controlled in producing a uniform thickness of up to several mils; however, such electroless plating process is more time-consuming than the electrolytic process. For purposes of the present invention, either the electrolytic plating or the electroless plating process may be utilized in forming the conductive bumps 130 and conductive bumps 132.

Thus, the electrolytic plating process employs an electrochemical plating process for depositing a conductive material. Likewise, the electroless plating process employs a chemical plating process. The conductive materials utilized in the electrolytic plating and electroless plating processes may include a base layer of tin or nickel followed by a gold layer, or plated layers of tin/silver/copper and alloys thereof. Other conductive materials may be utilized in the plating process in various

combinations of plated layers as known in the art such as, for example, copper, nickel, chromium, zinc, brass, cadmium, silver, lead, tin and gold and alloys thereof.

It is noted that conductive bumps 130 may be formed or coated with a surface finish or coating comprising a compliant, deformable or compressible material to help relax coplanarity requirements for conductive bumps 130 and 132. If such a surface finish is employed, slight compression of a semiconductor die 140 (see FIG. 5) against conductive bumps 130 or compression of interposer substrate 110 against a carrier substrate such as a printed circuit board (not shown) will bring the outer ends or tips of conductive bumps 130, 132 of somewhat different heights into coplanarity at a common level without damage to the conductive bumps 130, 132 or to other elements of semiconductor die 140 or interposer substrate 110. Suitable surface finish materials for providing some relaxation of coplanarity issues include, without limitation, gold, a conductive or conductor-filled polymer, or PbSn solder. Of course, gold may be plated as part of the bump plating process, as may consecutive layers of tin and lead, while a polymer or a solder paste may be applied to the surfaces of conductive bumps 132 after formation thereof.

In an alternative embodiment also depicted in FIG. 3A, the electrolytic plating or electroless plating processes may be limited to forming the conductive bumps 130 in their entireties. In other words, the plating process may not fill the through holes 116 to sufficiently form the conductive bumps 132 in the time taken for entirely forming the conductive bumps 130. In this case, the through holes 116 may be filled with a conductive paste 138, such as a solder paste. Preformed conductive bumps 132 may then be disposed in the conductive paste 138 so that the conductive bumps 132 slightly protrude from the second surface 114 of the interposer substrate 110 as a second level interconnect to correspond to and interconnect with a terminal pad pattern of a circuit board, other carrier substrate, or another semiconductor assembly. The preformed conductive bumps 132 used in this alternative may comprise any conductive material, such as solder balls. Further, a conductive paste 138 may be used to fill through holes 116 without prior plating, if desired.

Turning to FIG. 4, a partial cross-sectional view of the interposer substrate 110 of the present invention and a semiconductor die 140 in a mutually superimposed, but not yet assembled position, is illustrated. The interposer substrate 110 includes the

conductive bumps 130 and conductive bumps 132 formed on and extending from the respective first surface 112 and second surface 114 thereof. The semiconductor die 140 includes an active surface 142 and a back surface 144 with an array of bond pads 146 on the active surface 142 thereof. The semiconductor dice 140 utilized in the present invention are bare, bumpless semiconductor dice and, more specifically, the active surfaces 142 of the semiconductor dice 140 do not include conductive bumps 130 formed on or bonded to the bond pads 146 thereof. As shown, individual semiconductor dice 140 may be assembled with individual interposer substrates 110.

In the unassembled position, the conductive bumps 130 on the interposer substrate 110 are positioned and aligned with the bond pads 146 on the semiconductor die 140 in preparation for a first level interconnect. Such positioning and aligning of the semiconductor die 140 to the conductive bumps 130 of the interposer substrate 110 may be accomplished with mechanically or optically referenced pick and place equipment, as is well known in the art.

FIG. 5 illustrates the semiconductor die 140 mounted to the interposer substrate 110 so that the bond pads 146 interconnect with the conductive bumps 130 formed on the interposer substrate 110. Such an interconnection forms a gap between the semiconductor die 140 and interposer substrate 110, wherein a dielectric flowable filler material 150 may be dispensed from dispenser head 152 to fill the gap. Prior to dispensing the dielectric filler material, the conductive bumps 130 and bond pads 146 may be bonded in a suitable process for the material or materials of conductive bumps 130. For example, if a plated bump with a thin gold coating is used for conductive bumps 130, thermosonic bonding may be used to interconnect conductive bumps 130 with bond pads 146. Heat-induced bump reflow may be used if conductive bumps are formed of a tin/lead, silver, or other solder material. Eutectic bonding may also be employed. The dielectric flowable filler material 150 may then be dispensed to fill the gap by any known method in the art, such as, for example, capillary action or by positive pressure from dispenser head 152, with optional application of a negative pressure (vacuum) to the gap at a location opposite dispenser head 152.

FIGS. 6 and 7 illustrate an alternative method of providing dielectric flowable filler material 150 between the semiconductor die 140 and the interposer substrate 110. Specifically, a nonconductive film (NCF) 154, which is nonflowable, is positioned on the interposer

substrate 110 over first surface 112. The nonconductive film 154 may comprise an adhesive resin to facilitate attaching the nonconductive film 154 to the semiconductor die 140 or interposer substrate 110, after which the semiconductor die 140 may be mounted to the interposer substrate 110 in a manner similar to that described above. In the mounting process, the conductive bumps 130 are caused to pierce through the nonconductive film 154 by application of pressure and heat to the semiconductor die 140 and interposer substrate 110 to make contact with the bond pads 146 on the semiconductor die 140. The conductive bumps 130, if formed of solder, may then be heated to a higher temperature to undergo a reflow process for bonding to the bond pads 146 on the semiconductor die 140. The nonconductive film 154 utilized in this alternative method may include a suitable nonflowable filler material as known in the art, such as, for example, a UF 511 or UF 527 nonconductive film (NCF), each manufactured by Hitachi Chemical, Semiconductor Material Division, Japan.

As another alternative to a flowable filler material or an NCF, an anisotropic conductive film (ACF) wherein conductivity is restricted to the Z-axis perpendicular to the plane of the film may be employed. In such an instance, the conductive bumps 130 need not pierce the ACF, as the bond pads 146 and conductive bumps 130 will be placed in electrical contact through mutually laterally insulated conductive elements carried by the dielectric portion of the ACF and extending therethrough transverse to the plane of the film. A suitable ACF includes an FC 212K or FC 262B film from Hitachi Chemical, Semiconductor Material Division, Japan.

As another approach, an NCF may be provided over the active surface 142 of the semiconductor die 140 and other unsingulated dice at the wafer level. The wafer having the NCF disposed thereon may then be singulated into individual semiconductor dice, which then may be mounted face down on the interposer substrate 110 so that the conductive bumps 130 pierce the nonconductive film 154 and mechanically and electrically contact the bond pads 146 on the singlulated semiconductor dice 140, in a manner similar to that previously described. In a similar manner, an ACF may be applied at the wafer level.

Turning to FIG. 8, a top plan view of a multiple die site interposer substrate 1110 with multiple semiconductor dice 140 attached thereto is illustrated. The interposer substrate 1110 includes multiple die attach sites 160 in a matrix of columns

and rows. Each die attach site 160 is configured to receive a semiconductor die 140 and includes the conductive bumps 130, conductive lines 120 and through holes 116 as previously set forth herein. Broken lines 162 are depicted to indicate where the interposer substrate 1110 may be separated into individual semiconductor assembly packages including individual interposer substrates 110 in a singulation process. The singulation process may be accomplished by sawing, by laser or electrodischarge machining or by any known separation or singulation process. Of course, as noted above, assembly of individual interposer substrates 110 with individual semiconductor dice 140 is also contemplated as within the scope of the present invention.

FIG. 9 illustrates an individual semiconductor assembly package 170 with an encapsulation material 172 formed thereon. Either prior to or subsequent to the singulation process, if a plurality of semiconductor dice 140 is connected to a multiple die site interposer substrate 1110, a dielectric encapsulation material 172 may be provided over each of the semiconductor dice 140 and its associated interposer substrate 110. The encapsulation material 172 may be provided by any known process, such as transfer molding, injection molding or pot molding. The encapsulation material 172 provides environmental protection to the semiconductor die 140. A dielectric flowable filler material 150 or a nonconductive film 154 may also be employed, as desired, prior to encapsulation. It is specifically noted that adequate clearance may be provided between die sites on an interposer substrate 1110 so that a blanket deposition of molding compound on the first surface 112 of interposer substrate 1110 may be employed to encapsulate the back sides and sides of all semiconductor dice attached thereto, followed by singulation of individual assemblies of semiconductor dice 140 with associated interposer substrates 110 along broken lines 162, as by sawing.

Thus, according to the present invention, interposer substrate 110 provides conductive bumps 130 formed on the first surface 112 thereof to provide a first level interconnect to bond pads 146 of a semiconductor die 140. Additionally, interposer substrate 110 provides conductive bumps 132 on the second surface 114 thereof to provide a second level interconnect to a carrier substrate or another semiconductor assembly. With this arrangement, the conventional step of wafer bumping is eliminated by providing the conductive bumps 130 on the interposer substrate 110. Therefore, it can be well appreciated by a person of ordinary skill in the art that if the conductive

bumps 130 on an interposer substrate 110 are faulty, the cost of replacing the interposer substrate 110 is substantially less than the replacement of semiconductor dice having faulty bumps. In other words, semiconductor dice are more costly to replace than the interposer substrate 110. Furthermore, simultaneously forming the conductive bumps 132 and conductive bumps 130 on the interposer substrate 110 is cost effective and simplifies the assembly and fabrication process. Further, the present invention may be used to eliminate the use of solder balls, thereby providing a lead-free assembly.

FIG. 10 illustrates a multilevel interposer substrate 210, according to a second embodiment of the present invention. In the second embodiment, the interposer substrate 210 includes a first surface 212 and a second surface 214 with recesses 216 formed in the second surface 214 thereof. Similar to the first embodiment, conductive lines 220 may be formed over the first surface 212. In addition, the interposer substrate 210 includes additional conductive line connections 228 at multiple levels within the interposer substrate 210, which interconnect to the conductive lines 220 on the first surface 212. Conductive bumps 230 may be formed on the conductive lines 220 on the first surface 212 by a plating process as set forth with respect to the first embodiment. Conductive bumps 232 may also be formed in the recesses 216 on the second surface 214 through the plating process, simultaneously with conductive bumps 230. In the alternative, after forming the conductive bumps 230, a conductive paste and conductive ball, such as a solder ball, may be disposed in the recesses 216 on the second surface 214 of the interposer substrate 210. A portion of recesses 216 may, of course, be plated during formation of conductive bumps 230.

FIG. 11 illustrates the interposer substrate 210 of the second embodiment with multiple semiconductor dice 240 mounted thereon by conductive bumps 230 on bond pads 246 to form a multi-die package 270. The semiconductor dice 240 may be underfilled with a dielectric filler material 250 or an NCF 254 and encapsulated with an encapsulation material 272 for environmental protection of the semiconductor dice 240, as previously set forth with respect to the first embodiment.

In the second embodiment, it can be well appreciated by one of ordinary skill in the art that the multiple levels of conductive lines 220 in the interposer substrate 210 may facilitate the assembly of multiple semiconductor dice 240 in a single package to form, for example, a multi-chip memory module or a multi-chip module including

different types of semiconductor dice. Further, in a manner similar to the first embodiment, interposer substrate 210 includes the conductive bumps 230 and the conductive bumps 232 on the respective first surface 212 and second surface 214 to provide a respective first level interconnect and second level interconnect. It is also contemplated that fabrication of a multi-chip module using a single level interposer substrate 110 lies within the scope of the present invention and that the use of conductive lines 220 on both first and second surfaces 112, 114 of an interposer substrate 110 may be particularly suitable for fabrication of such a multi-chip module.

As illustrated in block diagram form in drawing FIG. 12, semiconductor assembly package 170 or 270 of the first and second embodiments or equivalents thereof may be respectively mounted to a circuit board 310 in an electronic system 300, such as a computer system. In the electronic system 300, the circuit board 310 may be connected to a processor device 320, which communicates with an input device 330 and an output device 340. The input device 330 may comprise a keyboard, mouse, joystick or any other type of electronic input device. The output device 340 may comprise a monitor, printer or storage device, such as a disk drive, or any other type of output device. The processor device 320 may be, but is not limited to, a microprocessor or a circuit card including hardware for processing instructions for the electronic system 300. Additional structure for the electronic system 300 is readily apparent to those of ordinary skill in the art.

Thus, it will be readily apparent to those of ordinary skill in the art that the present invention provides a simple, robust and economical interposer substrate and resulting packaged semiconductor die or dice. The bumping of an interposer substrate enables discarding of defective interposer substrates before attachment of a semiconductor die thereto and thus eliminates scrapping of assemblies due to defective interconnects. Further, the capability of forming bumps on both sides of an interposer substrate by simultaneous plating thereof speeds the interposer fabrication process and results in exact bump placement and precise bump dimensioning. The elimination of wafer bumping with solder balls by use of the present invention also speeds up the die fabrication process and eliminates defective bumping concerns with respect to the wafer. Furthermore, the present invention enables reduction in package thickness in comparison to solder-bumped assemblies and a further reduction in thickness through

the use of bumps disposed in through holes or vias. Even if solder balls are employed for the second level interconnect, placement thereof is facilitated by the presence of the through holes or vias in which the solder balls may be disposed, as is a reduction in package thickness by recessing of a portion of the solder balls.

While the present invention has been disclosed in terms of certain currently preferred embodiments and alternatives thereof, those of ordinary skill in the art will recognize and appreciate that the invention is not so limited. Additions, deletions and modifications to the disclosed embodiments may be effected without departing from the scope of the invention as claimed herein. Similarly, features from one embodiment may be combined with those of another while remaining within the scope of the invention.

CLAIMS

What is claimed is:

1. A method of forming an interposer substrate having a first level interconnect and a second level interconnect, the method comprising:

plating conductive bumps associated with a first major surface of a substantially planar interposer substrate body in a pattern for the first level interconnect and conductive bumps associated with a second major surface of the interposer substrate body in a pattern for the second level interconnect to at least one conductive line carried by the interposer substrate body, plating comprising plating the conductive bumps associated with at least one of the first major surface and the second major surface in at least some through holes of a plurality of through holes in the interposer substrate body;

providing conductive paste within at least one through hole of the plurality of through holes; and

providing a conductive ball at least partially within the conductive paste, the conductive ball protruding from at least one of the first major surface and the second major surface of the interposer substrate body.

2. The method of claim 1, wherein plating conductive bumps comprises simultaneously plating the conductive bumps associated with the first major surface and the conductive bumps associated with the second major surface.

3. The method of claim 1, further comprising forming a plurality of conductive lines over at least one of the first major surface and the second major surface of the interposer substrate body and extending between at least one through hole of the plurality of through holes and at least one of the conductive bumps associated with at least one of the first major surface and the second major surface of the interposer substrate body.

4. The method of claim 1, wherein plating comprises at least one of an electrolytic plating process and an electroless plating process.

5. The method of claim 4, wherein plating further comprises plating the conductive bumps associated with the first major surface and the conductive bumps associated with the second major surface from conductive materials comprising at least one of copper, nickel, chromium, zinc, brass, cadmium, silver, tin and gold.

6. The method of claim 4, wherein plating further comprises forming at least some of the conductive bumps associated with the first major surface and the conductive bumps associated with the second major surface from multiple layers of conductive materials comprising at least one of copper, nickel, chromium, zinc, brass, cadmium, silver, tin, lead and gold.

7. The method of claim 2, wherein simultaneously plating comprises configuring the conductive bumps associated with the first major surface to protrude from the first major surface of the substantially planar interposer substrate body.

8. The method of claim 7, further comprising disposing a preformed conductive element on at least some of the conductive bumps plated in the at least some through holes of the plurality of through holes to cause each preformed conductive element to protrude from at least one of the first major surface and the second major surface of the substantially planar interposer substrate body.

9. The method according to claim 1, wherein plating further comprises forming at least one of the conductive bumps associated with one of the first major surface and the second major surface laterally abutting an end of the at least one conductive line.

10. A method of assembling a semiconductor device assembly, the method comprising:

plating conductive bumps associated with a first major surface of an interposer substrate and conductive bumps associated with a second major surface of the interposer substrate to at least one conductive line carried by the interposer substrate, plating comprising plating the conductive bumps associated with at least one of the first major surface and the second major surface in at least some through holes of a plurality of through holes extending through the interposer substrate;

providing conductive paste within at least one through hole of the plurality of through holes;

providing a conductive ball at least partially within the conductive paste, the conductive ball protruding from at least one of the first major surface and the second major surface of the interposer substrate; and

electrically connecting bond pads of at least one semiconductor die to the conductive bumps associated with at least one of the first major surface and the second major surface of the interposer substrate.

11. The method of claim 10, further comprising disposing a dielectric filler material between the at least one semiconductor die and the interposer substrate.

12. The method of claim 11, wherein disposing dielectric filler material comprises dispensing the dielectric filler material in flowable form to fill a gap between the at least one semiconductor die and the interposer substrate.

13. The method of claim 11, wherein disposing dielectric filler material comprises disposing a nonflowable dielectric filler material between the at least one semiconductor die and the interposer substrate.

14. The method of claim 13, further comprising selecting the nonflowable dielectric filler material from the group consisting of a nonconductive film and an anisotropically conductive film.

15. The method of claim 10, wherein electrically connecting bond pads of at least one semiconductor die to the conductive bumps comprises electrically connecting bond pads of each of a plurality of semiconductor dice to the conductive bumps associated with at least one of the first major surface and the second major surface of the interposer substrate.

16. The method of claim10, further comprising encapsulating a back surface of the at least one semiconductor die with an encapsulation material.

17. A method of forming an interposer substrate having a first level interconnect and a second level interconnect, the method comprising:

providing a substantially planar interposer substrate body having a first major surface and a second major surface;

providing at least one conductive line carried by the interposer substrate body;

forming at least one through hole through the interposer substrate body to the at least one conductive line;

plating at least one conductive bump associated with the first major surface of the interposer substrate body to the at least one conductive line;

providing conductive paste within the at least one through hole; and

providing a conductive ball at least partially within the conductive paste, the conductive ball protruding from the second major surface of the interposer substrate body.

18. The method of claim 17, wherein plating at least one conductive bump comprises:

plating a first conductive bump to a first surface of the at least one conductive line; and

plating a second conductive bump to a second surface of the at least one conductive line;

wherein providing conductive paste comprises providing the conductive paste within the at least one through hole over the second conductive bump.

19. The method of claim 18, wherein plating at least one conductive bump comprises simultaneously plating the first conductive bump and the second conductive bump.