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ORIGINAL
COMPLETE SPECIFICATION
STANDARD PATENT

Invention Title:

"TONE DETECTOR"

The following statement is a full description of
this invention, including the best method of
performing it known to us:-

1-20031133

This invention relates to tone detection and in particular to an improved arrangement which allows a relatively low cost microprocessor to detect the presence or absence of particular frequencies within an incoming signal, such as, for example dial tone or call waiting tone received from exchange equipment by a telephone subset .

5 Several tone detector methods are known. One method comprises the steps of passing the signal containing the tone to be detected through a very high Q bandpass filter, a level shifter and then into a digital input port of a microprocessor. The microprocessor will see a square wave at the input pin whenever the required frequency is present in the input signal. This can easily be detected by interrupts or polling.

10 In this method, however, the filter tends to be relatively expensive, usually using several stages to give the desired roll-off and incorporating tight-tolerance or factory-tuned components for centre-frequency accuracy.

Another known method is to incorporate a phase-locked loop (PLL). In this case, the input signal is passed through a low-Q bandpass filter, into the PLL and the Lock
15 signal from the PLL is connected to a digital input port of a microprocessor.

This method is also relatively expensive, and PLL being a significant component of the cost. It still requires tight tolerance or factory-tuned components for centre-frequency accuracy.

Another known method which is less costly than the previously mentioned method
20 passes the input signal through a low-Q bandpass filter and a level shifter into a digital input port of a microprocessor. The microprocessor will see a squared off version of the filtered input signal. If the microprocessor is interrupted on every rising (or falling) edge it can time the period between edges. If the period corresponds to the search frequency (or one of the search frequencies) then the microprocessor can indicate the presence of
25 the signal. Typically though, many matching samples would need to occur before the signal could be detected with any certainty. This method is quite sensitive to input noise.

This method uses relatively cheap components to provide a means of detecting multiple frequencies with a reasonably tight bandwidth. However, depending on the microprocessor, this method could use a significant proportion of the available
30 processing power.

Digital signal processors designed specifically for tone detection are also known,

but are relatively expensive.

It is an object of the present invention to provide an improved tone detector arrangement in which tight bandwidth is achieved at relatively low cost.

5 It is a further object of the present invention to provide an improved tone detector arrangement which the tight bandwidth is achieved with minimum processing power.

According to the invention there is provided a tone detector arrangement comprising an analog signal input means coupled to a digital input port of a microprocessor via a bandpass filter means and an analog-to-digital converter means, wherein said microprocessor includes sampling means for sampling signals applied to
10 said analog signal input means, n-bit buffer means for storing data representing sampled signals, and an analysis means for periodically analysing samples in said buffer means, said analysis means using a modified Fourier Transform to detect signals of a predetermined frequency.

15 In order that the invention may be readily carried into effect, embodiments thereof will now be described in relation to the accompanying drawings, in which:

Figure 1 shows a first embodiment of the invention.

Figure 2 shows a record embodiment of the invention.

Figure 3 is a flow chart of actions executed in the sampler over analyser shown in Figures 1 - 2.

20 Referring to Figure 1, the arrangement comprises a bandpass filter to filter out most of the noise and extraneous signal from the input signal prior to being sampled by the microprocessor.

A limiter to convert the analog input signal into a digital signal useable by the microprocessor and also to filter out low power noise signals. Negative input voltages
25 are shifted to a digital LOW level. Positive noise voltages above the threshold are shifted to a digital HIGH level. A small amount of hysteresis prevents the system from falsely triggering on low level signals.

An algorithm used by the microprocessor detects specific frequencies, the algorithm is divided into two parts. The first part samples the input signal and stores it in
30 a buffer for later analysis. Sampling must take place at a relatively high frequency, but the instruction count per sample is low. The second part, the analysis section,

periodically analyses the sampled information for the presence of the specified frequency. This requires more processing time per period but can usually be performed at a much lower frequency.

5 The microprocessor regularly samples the status of the input pin and shifts the sample into an n-bit buffer. This section is time critical.

10 Normally, in digital signal processing, the sampling frequency needs to be about 3 or 4 times higher than the bandwidth of the input signal. However, in this application under-sampling may be used. The designer must make sure though, that the bandpass filter is capable of discriminating between the target frequency and any alias frequency introduced by the sampling rate.

For example: if searching for a 450 Hz signal, then a sampling rate of 1500 Hz would detect a signal with a frequency of 1050 Hz. This example therefore requires a bandpass filter centred at 450 Hz which will attenuate any signal at 1050 Hz to below the noise threshold.

15 In another example: if searching for a 2130 Hz signal , then a sampling rate of 1626.6 Hz would give alias frequencies at 503 Hz, 1123 Hz, 2750 Hz, etc. This example requires a bandpass filter centred at 2130 Hz which will attenuate these frequencies to below the noise threshold.

20 The size of the sample buffer, n , depends only on the bandwidth desired and the sample rate according to the following formula.

$$\text{Buffer size} = \text{Sample Rate} / \text{Bandwidth}$$

For example, if a bandwidth of 30 Hz is required while sampling at 1500 Hz, 50 samples would need to be stored.

25 An analysis section periodically examines the samples that have been made to determine whether a particular frequency is present in the input signal. This section is not time critical.

The algorithm used in this section is based on the standard Fourier Transform, however a number of modifications have been made to adapt it to a simple low-cost microprocessor.

30 The formula for the Fourier Transform is as follows:

$$F(\omega) = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{\infty} f(t) e^{-\omega t} dt$$

and theory states that the component of energy in a signal, $f(t)$, at the radial velocity, ω , is given by the magnitude $|F(\omega)|$. In practice, the complex exponential term is usually treated as the sum of a cosine term and an imaginary sine term.

In order to be used on a simple microprocessor this invention simplifies this formula in the following ways:

1. Instead of an analog input signal, the input is treated as a sampled 1-bit digital signal. The sample is 0 if the input signal is negative and 1 if it is positive. (In this algorithm, the value 0 really represents -1).
2. Instead of multiplying by $\sin(\omega t)$ and $\cos(\omega t)$ the arrangement of the present invention multiplies by two orthogonal square waves at the detection frequency.
3. Instead of multiplication, the arrangement uses bitwise exclusive-NOR (or exclusive -OR).
4. Instead of integrating over eternity, the last n samples are simply summed over. The sum simplifies to a count of the number of '1' bits in the result.
5. Any constants are ignored.
6. Instead of adding the two orthogonal components together using Pythagorean addition, the arrangement simply takes the absolute value and adds the two components together.

Referring to Figure 3, pseudocode and a flowchart for the analysis section follows:

1. Start (periodically).
2. Temp1 = Samples xor squarewave (Temp1 is an n -bit buffer)
Temp2 = Samples xor orthogonal squarewave (Temp2 is an n -bit buffer)
3. Bits1 = Number of 1 bits in Temp1
Bits2 = Number of 1 bits in Temp2
4. Value1 = absolute value of $(n/2 - \text{Bits1})$
Value2 = absolute value of $(n/2 - \text{Bits2})$
5. Result = Value1 + Value2

6. If Result is greater than Threshold then

frequency is present

else

frequency is not present

5 Referring to Figure 2, in a further embodiment of the present invention, a digital divide-by-n circuit is interposed between the level shifter and the microprocessor. This modification allows the arrangement to detect the presence of frequencies that would otherwise require more processing power. Software in the microprocessor is arranged to look for a signal that has a frequency 1/mth of the search frequency.

10 This modification also affects the relationship between bandwidth, sample rate and buffer size:

$$\text{Buffer size} = (\text{Sample Rate} / \text{Bandwidth}) \cdot m$$

Because the algorithm performs an analysis based on a large number of input samples, the algorithm is relatively insensitive to small amounts of noise.

15 However, because of the characteristics of the limiter circuit, if a noise signal more than 3dB above the search frequency passes through the bandpass filter, the algorithm will not be able to detect the search frequency.

Preferably, in high noise environments, the bandpass filter should be made as narrow as practicable.

20 Adding a divider also significantly reduces the noise performance of the algorithm. In high noise environments, preferably the divider should not be used.

This invention has an application wherever a low cost microprocessor is used to detect the presence of a particular frequency within an incoming signal, and may be used, for example:

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1. In telephones to discriminate between different dial tones.
 2. In telephones to detect the presence of call waiting or CIDCW tones.
 3. In pay phones to detect the presence of metering pulses.
 4. Electricity supply off-peak signal detection.
 5. FM radio 19-kHz carrier detection.

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The arrangement may be implemented purely in hardware (for example, in an integrated circuit) as a dedicated tone detector for each of the above applications.



The claims defining the invention are as follows:

1. A tone detector arrangement comprising an analog signal input means coupled to a digital input port of a microprocessor via a bandpass filter means and an analog-to-digital converter means, wherein said microprocessor includes sampling means for sampling signals applied to said analog signal input means, n-bit buffer means for storing data representing sampled signals, and an analysis means for periodically analysing samples in said buffer means, said analysis means using a modified Fourier Transform to detect signals of a predetermined frequency.
2. An arrangement as claimed in claim 1, wherein a digital divide-by-n circuit means is operatively interposed between said converter means and said digital input port of the microprocessor.
3. An arrangement as claimed in claim 1 or 2, incorporated in a telephone subset.
4. An arrangement substantially as herein described with reference to Figures 1 - 2 of the accompanying drawings.

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