What is claimed is:

1. A semiconductor device, comprising:

an active pattern disposed on a substrate;

a gate structure disposed on the active pattern;

channels disposed on the substrate, where the channels are spaced apart from each other in a vertical direction that is substantially perpendicular to an upper surface of the substrate;

a first epitaxial layer disposed on a portion of the active pattern adjacent to the gate structure; and

a contact plug disposed on the first epitaxial layer, wherein the contact plug includes:

a lower portion;

a middle portion disposed on the lower portion, wherein the middle portion has a width that increases along the vertical direction from a bottom to a top thereof; and

an upper portion disposed on the middle portion,

wherein a width of the lower portion of the contact plug is substantially constant in the vertical direction, and a width of an upper surface of the middle portion of the contact plug is greater than a width of a lower surface of the upper portion of the contact plug.

2. The semiconductor device as claimed in claim 1, further comprising a second epitaxial layer disposed on the first epitaxial layer, wherein the second epitaxial layer contacts a sidewall of the upper portion of the contact plug.

3. The semiconductor device as claimed in claim 2, wherein the second epitaxial layer includes one of silicon or silicon doped with p-type impurities.

4. The semiconductor device as claimed in claim 2 or claim 3, further comprising:

a first ohmic contact pattern interposed between the contact plug and the first epitaxial layer; and

a second ohmic contact pattern interposed between the contact plug and the second epitaxial layer.

5. A semiconductor device, comprising:

an active pattern disposed on a substrate;

a gate structure disposed on the active pattern;

channels disposed on the substrate, where the channels are spaced apart from each other in a vertical direction that is substantially perpendicular to the upper surface of the substrate;

a first epitaxial layer disposed on a portion of the active pattern adjacent to the gate structure;

a contact plug that includes:

a lower portion and a middle portion sequentially stacked in the vertical direction, wherein the lower portion and the middle portion extend through an upper portion of the first epitaxial layer; and

an upper portion disposed on the middle portion, wherein the upper portion extends in the vertical direction; and

a second epitaxial layer disposed on the middle portion of the contact plug, wherein the second epitaxial layer contacts a portion of a sidewall of the upper portion of the contact plug,

wherein a width of the lower portion of the contact plug is substantially constant in the vertical direction, and a width of an upper surface of the middle portion of the contact plug is greater than a width of a lower surface of the upper portion of the contact plug.

6. The semiconductor device as claimed in claim 5, wherein the first epitaxial layer includes silicon doped with n-type impurities.

7. The semiconductor device as claimed in claim 5 or claim 6, wherein the second epitaxial layer includes one of silicon or silicon doped with p-type impurities.

8. A semiconductor device, comprising:

an active pattern disposed on a substrate, wherein the active pattern extends in a first direction that is substantially parallel to an upper surface of the substrate;

a gate structure on the active pattern, wherein the gate structure extends in a second direction that is substantially parallel to the upper surface of the substrate and crosses the first direction;

channels disposed on the active pattern and that are spaced apart from each other in a third direction that is substantially perpendicular to the upper surface of the substrate;

a first epitaxial layer disposed on a portion of the active pattern adjacent in the first direction to the gate structure, wherein the first epitaxial layer includes silicon doped with n-type impurities;

a contact plug disposed on the first epitaxial layer, wherein the contact plug includes:

a lower portion;

a middle portion disposed on the lower portion, wherein the middle portion has a width in the first direction that increases from a bottom to a top thereof along the

vertical direction; and

a upper portion disposed on the middle portion; and

a second epitaxial layer disposed on the middle portion of the contact plug, wherein the second epitaxial layer contacts a portion of a sidewall in the first direction of the upper portion of the contact plug and includes one of silicon or silicon doped with p-type impurities,

wherein a width of the lower portion of the contact plug is substantially constant in the vertical direction, and a width of an upper surface of the middle portion of the contact plug is greater than a width of a lower surface of the upper portion of the contact plug.