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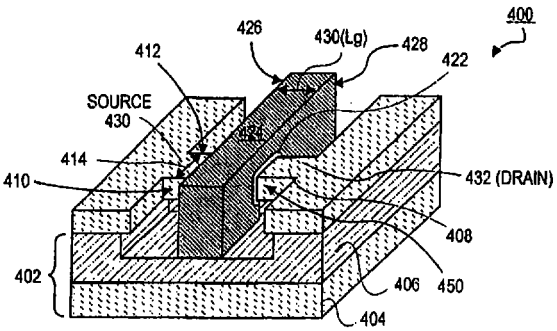
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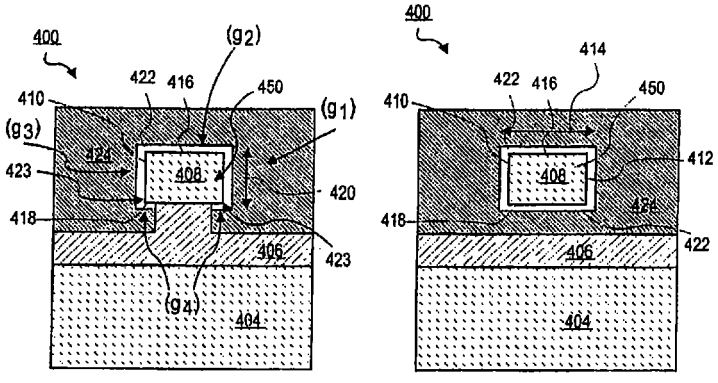
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(54) Title: NONPLANAR SEMICONDUCTOR DEVICE WITH PARTIALLY OR FULLY WRAPPED AROUND GATE ELECTRODE AND METHODS OF FABRICATION



A



B

C

(57) Abstract: A nonplanar semiconductor device and its method of fabrication is described. The nonplanar semiconductor device includes a semiconductor body having a top surface opposite a bottom surface formed above an insulating substrate wherein the semiconductor body has a pair laterally opposite sidewalls. A gate dielectric is formed on the top surface of the semiconductor body on the laterally opposite sidewalls of the semiconductor body and on at least a portion of the bottom surface of semiconductor body. A gate electrode is formed on the gate dielectric, on the top surface of the semiconductor body and adjacent to the gate dielectric on the laterally opposite sidewalls of semiconductor body and beneath the gate dielectric on the bottom surface of the semiconductor body. A pair source/drain regions are formed in the semiconductor body on opposite sides of the gate electrode.

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