

ABSTRACT OF THE DISCLOSURE

5 A VLSI integrated circuit (100), which comprises a
single IIR input and global section and identically-structured
cascadable filter sections (FS), each of which filter sections
includes a pair (102T,102B) of time-multiplexed, real-coefficient,
input-weighted FIR filter units and additional delay means, can be
selectively programmed to operate in any one of a number of
10 different filter configurations that can define real FIR or IIR
filters, complex FIR or IIR filters, or filters which are various
combinations thereof. One or more of such integrated circuits
(100) are useful for implementing a digital deghosting and/or
equalization filter.

This Sheet Has Been Replaced

