

Super-Halo Formation in FETs

Abstract

A semiconductor substrate has at least one PN junction with dopant atoms at the junction. A non-dopant at the junction provides interstitial traps to prevent diffusion during annealing. In a process for making this, a non-dopant diffusion barrier, e.g., C, N, Si, F, etc., is implanted into the "halo" region of a semiconductor device, e.g. diode, bipolar transistor, or CMOSFET. This combined with a lower annealing budget ("Spike Annealing") allows a steeper halo dopant profile to be generated. The invention is especially useful in CMOSFETs with gate lengths less than about 50 nm.

Fig 3