20030189342 7/03/03

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

CORRECTED VERSION

162162

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
4 April 2002 (04.04.2002)

PCT

(10) International Publication Number
WO 02/027473 A3

(51) International Patent Classification[7]: G06F 9/30

(21) International Application Number: PCT/US01/30318

(22) International Filing Date:
26 September 2001 (26.09.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/675,817 28 September 2000 (28.09.2000) US

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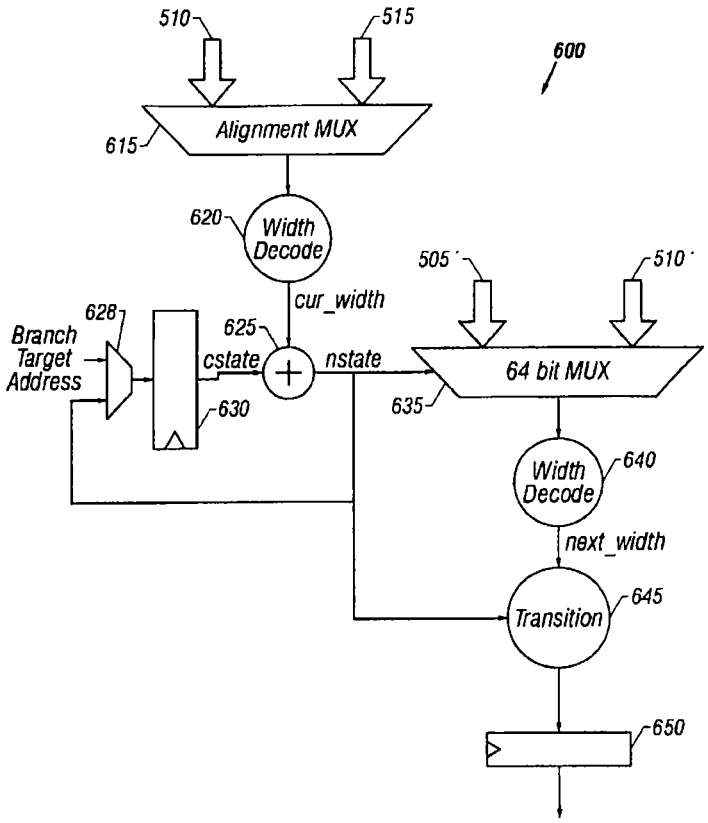
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(81) Designated States *(national)*: CN, JP, KR, SG.

Published:
— *with international search report*

[Continued on next page]

(54) Title: METHOD AND APPARATUS SUPPORTING VARIABLE LENGTH INSTRUCTION EXECUTION



(57) Abstract: In one embodiment, a digital signal processor includes look ahead logic to decrease the number of bubbles inserted in the processing pipeline. The processor receives data containing instructions in a plurality of buffers and decodes the size of a first instruction. The beginning of a second instruction is determined based on the size of the first instruction. The size of the second instruction is decoded and the processor determines whether loading the second instructions will deplete one of the plurality of buffers.

ACTION

WO 02/027473 A3

(88) **Date of publication of the international search report:**
22 August 2002

(48) **Date of publication of this corrected version:**
17 July 2003

(15) **Information about Correction:**
see PCT Gazette No. 29/2003 of 17 July 2003, Section II

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.