PROCESS FLOW FOR A PERFORMANCE ENHANCED MOSFET

WITH SELF-ALIGNED, RECESSED CHANNEL

ABSTRACT

A method for forming a self-aligned, recessed channel, MOSFET device that alleviates the problems due to short channel and hot carrier effects while reducing inter-electrode capacitance is described. A substrate with an active area encompassed by a shallow trench isolation (STI) region is provided. A mask oxide layer is then patterned and etched to expose the substrate and a portion of the STI region. The surface is etched and the mask oxide layer is eroded away while creating a gate recess in the unmasked area. A thin pad oxide layer is then grown overlying the surface followed by a deposition of a thick silicon nitride layer covering the surface and filling the gate recess. The top surface is planarized exposing the pad oxide layer. An additional oxide layer is grown causing the pad oxide layer to thicken. A portion of the silicon nitride layer is etched away and additional oxide layer is again grown causing the pad oxide layer to further thicken. This forms a tapered oxide layer along the sidewalls of the gate recess. The remaining silicon nitride layer is then removed, re-opening the gate recess. A threshold adjust and punch-through implantation is performed into the substrate below the gate recess. The pad oxide layer is then isotropically etched to remove the oxide layer at the bottom of the gate recess and a gate dielectric layer is grown in the bottom of the gate recess. Gate polysilicon is then deposited covering the top surface and filling the gate recess. The top surface is again planarized to expose the substrate. A screen oxide layer is then deposited, followed by light and heavy S/D implantations and annealing. Metalization and passivation complete the fabrication of the MOS transistor device.

Fig. 12A and Fig. 12B