SEMICONDUCTOR DEVICE AND PRODUCTION THEREOF

BACKGROUD OF THE INVENTION

This invention relates to a semiconductor device having a groove isolation structure with high reliability, and a process for producing the same.

As a process for electrically insulating isolation of adjacent elements on a semiconductor substrate, it is known a shallow groove isolation (SGI) process. According to the SGI process, shallow grooves are formed on a silicon substrate, followed by burying an oxide film thereinto by a chemical vapor deposition (CVD) method or a sputtering method. Since the SGI process has higher processing dimensional accuracy than a LOCOS structure conventionally used, it can provides a structure suitable for devices after a 0.25 μm process. But according to the SGI structure, since a burying oxide film is produced by a CVD method or a sputtering method, it has a density generally coarser than a thermally oxidized film (hereinafter referred to as "thermal oxide film"). Thus, about 5% shrinkage takes place during a subsequent thermal treatment step, resulting in formation of a void-like "cavity" at the interface of the oxide film even by slight etching using dilute hydrofluoric acid.

Fig. 2 is a cross-sectional view showing such a "cavity", wherein numeral 1 denotes a silicon

substrate, numeral 6 a burying insulating film or layer, and numeral 3 the "cavity".

When such a "cavity" is present, a wiring film or the like remains in the cavity at the time of patterning after a step of wiring and a deposition of an electrode film, resulting in often causing electrically undesirable phenomena such as short-circuit, etc.

In order to remove such a "cavity", S. Nag et al disclose in Tech. Dig. of IEEE, 1996, p. 841-844 that after burying a burying oxide film, thermal treatment is conducted in an oxidizing atmosphere to change Si in a groove into SiO_2 for reducing the volume, resulting in removing the "cavity".

But, according to this method, there arises an disadvantage in that a high mechanical stress is generated in the groove and adjacent silicon substrate portions due to about twice volume expansion of the oxide film as a side action of removal of "cavity".

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a semiconductor device having high reliability by making a generated stress lower than a critical stress and preventing generation of crystal defects or an increase of a junction leakage current, and a process for producing the same.

The present invention provides a semiconductor device comprising a semiconductor substrate having a

plurality of element formation regions and element isolation regions on a main surface thereof, each element isolation region comprising a groove formed in the semiconductor substrate, a thermal oxide film formed on the wall surface of the groove, and an insulating material buried in the groove, said thermal oxide film being formed while satisfying the formula:

$$D < 0.4^{(-100R + 7) - 1} (- 230\ T + 14.5) \qquad (1)$$

wherein D is a width of the element formation region (or active width); T is a thermal oxidation amount (thermal oxide film thickness) of the groove in terms of microns; and R is a curvature radius at an end bottom portion of the groove, provided that T is 0.01 μm or more.

The present invention also provides a process for producing a semiconductor device having a plurality of element formation regions and element isolation regions on a main surface of a semiconductor substrate, which comprises the steps of:

(a) forming a pad oxide film and a silicon nitride film on a semiconductor substrate, and removing a part of the semiconductor substrate from the portions wherein the element isolation regions are to be formed to form grooves, each groove having a curvature radius R at an end bottom portion of the groove,

(b) burying an insulating film in each groove to form a burying insulating film,

(c) forming a thermal oxide film on the wall surface of each groove while satisfying the following

formula:

$$D < 0.4^{(-100R + 7) - 1} (- 230\ T + 14.5) \quad (1)$$

wherein D is a width of the element formation region (or active width); T is a thermal oxidation amount of the groove in terms of microns; and R is a curvature radius at the end bottom portion of the groove, provided that T is 0.01 μm or more, and

(d) removing said burying insulating film, said silicon nitride film and said pad oxide film.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1A is a cross-sectional view for explaining the active width D, the curvature radius R at an end bottom portion of the groove; and the thermal oxidation amount T in terms of microns.

Fig. 1B is a graph showing a relationship between the thermal oxidation amount T (μm) and the active width D (μm).

Fig. 2 is a cross-sectional view for explaining a problem of prior art process.

Figs. 3A to 3G are cross-sectional views explaining one example of the process of the present invention for producing the semiconductor device.

Fig. 4 is a cross-sectional view for explaining the active width and the stress evaluation portion of a semiconductor device of the present invention.

Fig. 5 is a graph showing a relationship

between the shear stress and the active width of a semiconductor device of the present invention.

Fig. 6 is a cross-sectional view of one example of the semiconductor device of the present invention.

Fig. 7 is a plan view for explaining the definition of the active width in various embodiments in the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The present inventors have noticed causes for generating defects in the process for producing a semiconductor device having a groove isolation structure by the SGI process mentioned above, particularly mechanical scheme for generating high mechanical stress in the inside of the groove and neighboring portions in the silicon substrate, and studied how to remove such defects.

As a result, it was found that at end bottom portions of a groove, high stress was generated due to interference of volume expansion of the oxide film at the bottom of the groove and the side wall of the groove. Further, with an increase of the oxidation amount, this stress increased and often generated crystal defects such as dislocation in the silicon substrate. It was also found that when such crystal defects were generated in the transistor region, for example, there often caused an increase of junction

leakage current.

The present inventors found from various experiments that when an oxidation amount was constant, the crystal defects easily took place when the active width D (the distance between neighboring element isolation regions, that is, the width of element formation region) was large. Further, from a finite element method analysis simulating the above experiments, it was found that when the active width became larger, the stress generated also became larger, resulting in causing an increase of the junction leakage current at a certain critical stress or more. Thus, the present invention has been accomplished.

[Production of Semiconductor Device Having Groove Isolation Structure]

One example of producing a semiconductor device having a groove isolation structure is explained by the following steps (a) to (h) referring to Figs. 3A to 3G.

(a) A surface of a silicon substrate 1 is thermal oxidized to form a pad oxide film 2 with about 10 nm thick [Fig. 3A].

(b) On the pad oxide film 2, a silicon nitride film 4 having a thickness of about 150 nm is deposited [Fig. 3A].

(c) On the silicon nitride film 4, a photoresist 5 is formed [Fig. 3A].

(d) After removing the photoresist 5 on desired portions by a conventional light exposure method, a part of the silicon nitride film 4, a part of the pad oxide film 2, and a part of the silicon substrate 1 are removed by etching to form a shallow groove having an angle of about 100° at the upper end of the groove wall against the silicon substrate 1 [Fig. 3B]. At this time, a curvature radium R of about 50-60 nm or less is formed at an end portion of the groove.

(e) An insulating film such as a silicon oxide film (or a second silicon oxide film) is deposited by a chemical vapor deposition (CVD) method, a sputtering method, or the like and buried in the inside of the groove (hereinafter referred to as "burying insulating film" 6) [Fig. 3C].

(f) After depositing the burying insulating film 6, the silicon substrate 1 is subjected to oxidation at a temperature of about 1000°C in an oxidative atmosphere to conduct oxidation in the range of 10 to 65 nm in terms of the thickness of the resulting thermal oxide film 7 (or the first silicon oxide film), since the silicon oxide film produced by the CVD method or the sputtering method is generally a rough film [Fig. 3D].

(g) An excess portion of the burying insulating film 6 is etch backed using a chemical mechanical polishing (CMP) method or a dry etching method [Fig. 3E]. In this case, the silicon nitride film 4 used as an oxidation preventing film acts as an etching stopper

to prevent the silicon substrate 1 under the silicon nitride film 4 from etching [Fig. 3F].

(h) After removing the silicon nitride film 4 and the pad oxide film 2, the groove burying structure is completed. Then, a thermal oxide film 8, a gate electrode 9, a condenser electrode 19, a wiring 16, insulating films 15 and 17, etc. are formed thereon to complete the semiconductor device [Fig. 3G].

In Fig. 3G, numeral 10 denotes a side wall, numeral 11 a drain or source layer, numeral 12 a well layer, numeral 13 an insulating film, numeral 14 a plug, and numeral 18 a dielectric material film.

[Relation between Active Width and Properties]

The semiconductor thus produced was subjected to examination of a relation between the active width (the width of element formation region) D and physical properties such as junction leakage current and shear stress.

Table 1

Oxidation time	Active width			
	2 μm	4 μm	8 μm	16 μm
5 min.	o	o	X	X
10 min.	X	X	X	X

Table 1 shows the results of the active width dependency of junction leakage current when the oxidation time for the silicon substrate in the step (f) mentioned above [Fig. 3D] at 1000°C in an oxidative atmosphere is changed to 5 minutes and 10 minutes so as to change the active width of the MOS type transistor [see Fig. 4].

In Table 1, the mark o means that the junction current value is a permissible value or less, and the mark X means that the junction current value is over the permissible value.

As shown in Table 1, abnormal junction leakage current is generated when the active width is 8 μm or more in the case of oxidation time of 5 minutes. In the case of oxidation time of 10 minutes, abnormal junction leakage current is generated in all the active width.

Next, shear stress generated in the silicon substrate when the groove width was 1 μm was simulated and shown in Fig. 5. In Fig. 5, the abscissa axis shows an active width, and the ordinate axis shows shear stress at the end bottom portion of the groove. The stress evaluation position is shown in Fig. 4, which position is near the R portion at an end bottom portion of the groove.

In Fig. 5, the oxidation time of 5 minutes is shown by o and •, and the oxidation time of 10 minutes is shown by ■, wherein the mark o means that no abnormal junction leakage current is generated, and the marks •

and ■ mean that abnormal junction leakage current is generated.

As is clear from the results of Fig. 5, the generation of stress is dependent on the active width, and the active width becomes larger, the stress generated becomes larger. For example, when the oxidation time is 5 minutes, the shear stress becomes 850 MPa at the active width of 2 μm, 900 MPa at the active width of 4 μm and 950 MPa at the active width of 8 μm. When the oxidation time is 10 minutes, the shear stress is 950 MPa at the active width of 2 μm, and 1050 MPa at the active width of 4 μm or more. Further, from the plots • and ■ which mean generation of abnormal junction leakage current as shown in Table 1, it is admitted that abnormal junction leakage current takes place at the generation of shear stress of about 950 MPa.

[Relation among Active Width, Curvature Radius, and Thermal Oxidation Amount]

The active width D, the curvature radius R at the end bottom portion of groove, and the thermal oxidation amount T (thermal oxide film thickness) at the inner walls of the groove seem to be factors deciding the shear stress in the semiconductor having a SGI structure. Thus, the stress generated at the end bottom portion of the groove in the silicon substrate was analyzed by simulation by varying these factors

variously to obtain the relation when the shear stress is over 950 MPa.

The results are shown in Fig. 1B, wherein the abscissa axis shows the thermal oxide film thickness (T) and the ordinate axis shows the active width (D). In Fig. 1B, the results of the curvature radius R of 0.04 μm to 0.06 μm are shown. Further, the thermal oxide film thickness is taken from the value at the central portion of the groove width.

The regions wherein abnormal junction leakage current takes place are the regions above each linear line having larger active width. From Fig. 1B, it is recognized that with an increase of the oxidation amount, permissible active width becomes smaller, and with an decrease of the curvature radius, the permissible active width also becomes smaller.

The relation among the active width D (μm), the thermal oxide film thickness T (μm) and the curvature radius R (μm) at the end bottom portion of the groove shown in Fig. 1A is examined to obtain the following formula (1):

$$D < 0.4^{(-100R + 7) - 1} (- 230T + 14.5) \quad (1)$$

On the other hand, it is known experientially that the thermal oxidation amount T should be 0.01 μm or more in order to remove the "cavity" from the burying oxide film. Therefore, in the above formula (1), the thermal oxide film thickness T should be 0.01 μm or more in order to prevent the increase of junction leakage

current in the semiconductor device having the SGI structure.

Thus, the values of D, T and R should be determined to satisfy the formula (1) mentioned above.

The formula (1) is effective not only in the case of densified oxidation mentioned above, but also in the subsequent oxidations.

In the case of element isolation with the groove width of 0.25 μm or less as shown in Fig. 6, the angle of the groove against the surface of silicon substrate becomes about 100° substantially considering the coverage of the burying oxide film 6. Further, the depth of the groove is about 0.35 μm. From these values, the length at the bottom of the groove becomes about 0.126 μm. Thus, it becomes impossible to make the curvature radius R at the end bottom portion of the groove substantially 0.063 μm or more. From this value, the permissible active width (D) is calculated using the formula (1) to be about 16 μm, when the minimum oxidation amount (T) is 0.01 μm. In addition, permissible thermal oxidation amount (T) becomes 0.01 μm or more and less than 0.065 μm from Fig. 1B.

The element formation region in the present invention can take various shapes as shown in Fig. 7. In any case, the active width (D) means the maximum length in any shapes as shown in Fig. 7, for example.

The lower limit of the active width (D) is the minimum processing size, which is, for example, 0.25 μm

or more in general, but it is not impossible to be 0.1 μm or 0.05 μm.

The present invention is illustrated by way of the following Examples.

Example 1

On a silicon substrate, a pad oxide film of about 10 nm thick was formed by thermal oxidation at 800°C, followed by deposition of a silicon nitride film of about 150 μm thereon by a conventional method. A photoresist was formed on the silicon nitride film, and the photoresist was removed from the desired portions by a conventional light exposure method. Then, the silicon nitride film, the pad oxide film and a part of the silicon substrate under the removed photoresist were removed by etching to form shallow grooves. The curvature radius at the end bottom portion of the groove (R) was 0.05 μm.

Then, a silicon oxide film was deposited in the grooves by a CVD method to form a burying insulating film. Oxidation was carried out at about 1000°C in an oxidative atmosphere to form a thermal oxide film on the inner walls of the grooves.

The upper portion of the burying insulating film above the groove was etch backed by a CMP method, followed by removal of the silicon nitride film and the pad oxide film to complete a groove burying structure. Thereafter, gate electrodes, condenser electrodes,

wirings, insulating film were formed thereon to give a semiconductor device shown in Fig. 3G. The active width (D) was 2 μm, the thermal oxidation amount (thermal oxide film thickness) in the groove (T) was 0.03 μm. The values of R, T and D satisfied the formula (1) and no "cavity" was formed. There arose no problem at the time of patterning after formation of wirings and the electrodes. The junction leakage current was below the permissible value.

Comparative Example 1

A semiconductor device was produced in the same manner as described in Example 1 except for making R 0.05 μm, D 18 μm and T 0.03 μm.

The thus produced semiconductor device generated abnormal junction leakage current.

As mentioned above, according to the present invention, the semiconductor device having a groove isolation structure without leakage current abnormal can be produced easily and precisely.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising a semiconductor substrate having a plurality of element formation regions and element isolation regions on a main surface thereof, each element isolation region comprising a groove formed in the semiconductor substrate, a thermal oxide film formed on the wall surface of the groove, and an insulating material buried in the groove, said thermal oxide film being formed while satisfying the formula:

$$D < 0.4^{(-100R + 7) - 1} (-230\ T + 14.5) \quad (1)$$

wherein D is a width of the element formation region; T is a thermal oxidation amount of the groove in terms of microns; and R is a curvature radius at an end bottom portion of the groove, provided that T is 0.01 μm or more.

2. A semiconductor device having a plurality of element formation regions and element isolation regions on a main surface thereof, each element isolation region comprising a groove formed in the semiconductor substrate, a first silicon oxide film form on the wall surface of the groove by thermal oxidation, and a second silicon oxide film buried in the groove, said first silicon oxide film being formed while satisfying the formula:

$$D < 0.4^{(-100R + 7) - 1} (-\ 230\ T + 14.5) \quad (1)$$

wherein D is a width of the element formation region; T is a thermal oxidation amount of the groove in terms of

* C L M S *

microns; and R is a curvature radius at an end bottom portion of the groove, provided that T is 0.01 μm or more.

3. A semiconductor device according to Claim 1 or 2, wherein the thermal oxidation amount T is in the range of 0.01 μm or more and less than 0.065 μm.

4. A semiconductor device according to Claim 1 or 2, wherein the thermal oxidation amount T is in the range of 0.01 μm or more and less than 0.065 μm, and the width of the element formation region D is 16 μm or less.

5. A process for producing a semiconductor device having a plurality of element formation regions and element isolation regions on a main surface of a semiconductor substrate, which comprises the steps of:

(a) forming a pad oxide film and a silicon nitride film on a semiconductor substrate, and removing a part of the semiconductor substrate from the portions wherein the element isolation regions are to be formed to form grooves, each groove having a curvature radius R at an end bottom portion of the groove,

(b) burying an insulating film in each groove to form a burying insulating film,

(c) forming a thermal oxide film on the wall surface of each groove while satisfying the following formula:

$$D < 0.4^{(-100R + 7) - 1} (-230\ T + 14.5) \qquad (1)$$

wherein D is a width of the element formation region; T

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is a thermal oxidation amount of the groove in terms of microns; and R is a curvature radius at an end bottom portion of the groove, provided that T is 0.01 μm or more, and

(d) removing said burying insulating film, said silicon nitride film and said pad oxide film.

6. A process for producing a semiconductor device having a plurality of element formation regions and element isolation regions on a main surface of a silicon substrate, which comprises the steps of:

(a) forming a pad oxide film by thermal oxidation on a main surface of the silicon substrate,

(b) forming a silicon nitride film on the pad oxide film,

(c) forming a photoresist on the silicon nitride film,

(d) removing the photoresist film from the portions wherein said element isolation regions are to be formed, and also removing a part of the silicon nitride film, a part of the pad oxide film and a part of the silicon substrate from said portions to form each groove having a curvature radius R at an end bottom portion of the groove,

(e) burying an insulating material in the groove to form a burying insulating film,

(f) forming a thermal oxide film on the wall surface of each groove while satisfying the following formula:



$$D < 0.4^{(-100R + 7) - 1} (-230\ T + 14.5) \quad (1)$$

wherein D is a width of the element formation region; T is a thermal oxidation amount of the groove in terms of microns; and R is a curvature radius at an end bottom portion of the groove, provided that T is 0.01 μm or more, and

(g) removing excess burying insulating film, and

(h) removing the silicon nitride film and the pad oxide film.

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