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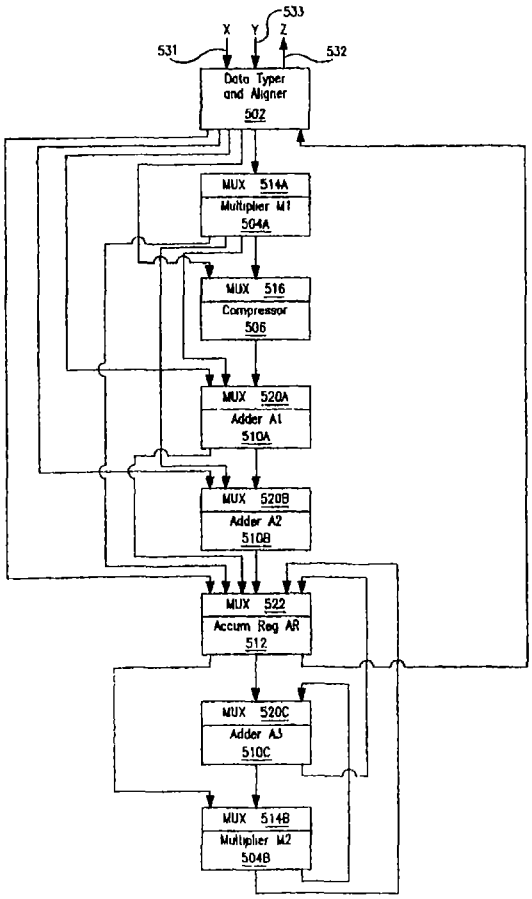
(54) Title: METHOD AND APPARATUS FOR INSTRUCTION SET ARCHITECTURE HAVING DYADIC DIGITAL SIGNAL PROCESSING INSTRUCTIONS



(57) Abstract: The instruction set architecture (ISA) for application specific signal processor (ASSP) is tailored to digital signal processing applications. The instruction set architecture implemented with the ASSP is adapted to DSP algorithmic structures The instruction word of the ISA is typically 20 bits but can be expanded to 40 bits to control two instructions to be executed in series or parallel All DSP instructions of the ISA are dyadic DSP instructions performing two operations with one instruction in one cycle. The DSP instructions or operations in the preferred embodiment include a multiply instruction (MILT) (504), an addition instruction (ADD)(510), a minimize/maximize instruction (MIN/MAX) also referred to as an extrema instruction, and a no operation instruction (NOP) each having an associated operation code ("opcode") The present invention efficiently executes DSP instructions by means of the instruction set architecture and the hardware architecture of the application specific signal processor

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