CLAIMS

1. A semiconductor package assembly, comprising:

a base plate, having a first surface, wherein the base plate comprises a first signal transmission region and a second signal transmission region that are respectively located on two opposite ends of the base plate, and the first signal transmission region and the second signal transmission region are not electrically connected to each other;

a first chip structure, located on the base plate and electrically connected to the first surface of the base plate;

an intermediary layer, having a first interconnection surface, wherein the first interconnection surface has a first interconnection region and a second interconnection region, a first solder ball is formed on the first interconnection region, a first pad is formed on the second interconnection region, and the intermediary layer is electrically connected only to the second signal transmission region of the base plate by means of the first pad; and

a molding compound, sealing the first chip structure, the intermediary layer and the first surface of the base plate, wherein the first solder ball has a surface exposed from the molding compound, and there is a preset height between the exposed surface of the first solder ball and the first interconnection surface of the intermediary layer.

2. The semiconductor package assembly of claim 1, wherein the first chip structure comprises a plurality of first semiconductor chips that are successively stacked in a direction perpendicular to the base plate; and wherein the intermediary layer is located on the first chip structure.

3. The semiconductor package assembly of claim 2, further comprising:

a first conductive wire, wherein each of the first semiconductor chips is electrically connected to the base plate by means of the first conductive wire; and

a second conductive wire, wherein the second interconnection region is electrically connected only to the second signal transmission region of the base plate by means of the second conductive wire.

4. The semiconductor package assembly of claim 2, wherein a plurality of second pads are formed on the first interconnection region; a number of the first pads is greater than a number of the second pads; and an area of the first pad is less than an area of the second pad.

5. The semiconductor package assembly of claim 1, further comprising:

a second package structure, comprising a second solder ball and electrically connected to the first solder ball by means of the second solder ball.

6. The semiconductor package assembly of claim 5, wherein a volume of the first solder ball is greater than a volume of the second solder ball.

7. The semiconductor package assembly of claim 5, wherein the molding compound has a first thickness in a direction perpendicular to the base plate; and

wherein the second package structure comprises a second molding compound; the second molding compound has a second thickness in the direction perpendicular to the base plate; and the first thickness is greater than or equal to the second thickness.

8. The semiconductor package assembly of claim 1, wherein the preset height is not less than 1/5-1/2 of a thickness of the intermediary layer.

9. The semiconductor package assembly of claim 1, wherein the base plate further includes a third signal transmission region located between the first signal transmission region and the second signal transmission region, and the first chip structure is located on the third signal transmission region.

10. A method for manufacturing a semiconductor package assembly, comprising:

providing a base plate, wherein the base plate has a first surface, the base plate comprises a first signal transmission region and a second signal transmission region that are respectively located on two opposite ends of the base plate, and the first signal transmission region and the second signal transmission region are not electrically connected to each other;

forming a first chip structure on the base plate, wherein the first chip structure is electrically connected to the first surface of the base plate;

forming an intermediary layer, wherein the intermediary layer has a first interconnection surface, the first interconnection surface has a first interconnection region and a second interconnection region, a first solder ball is formed on the first interconnection region, a first pad is formed on the second interconnection region, and the intermediary layer is electrically connected only to the second signal transmission region of the base plate by means of the first pad; and

forming a molding compound, wherein the molding compound seals the first chip structure, the intermediary layer and the first surface of the base plate, the first solder ball has a surface exposed from the molding compound, and there is a preset height between the exposed surface of the first solder ball and the first interconnection surface of the intermediary layer.

11. The method of claim 10, wherein the forming a molding compound comprises:

forming a first packaging mold, wherein a surface of the first packaging mold is parallel to a surface of the base plate, and the first packaging mold is located above the first chip structure and the intermediary layer, and there is a certain distance from the first packaging

mold to the first chip structure and the intermediary layer;

forming a molding compound pre-layer by using the first packaging mold as a mask; and

removing part of the molding compound pre-layer to form the molding compound and expose a surface of the first solder ball.

12. The method of claim 10, wherein the forming a first chip structure comprises:

forming a plurality of first semiconductor chips that are successively stacked in a direction perpendicular to the base plate; and

wherein the intermediary layer is formed on the first chip structure.

13. The method of claim 12, further comprising: after forming the intermediary layer,

forming a first conductive wire, wherein each of the first semiconductor chips is electrically connected to the base plate by means of the first conductive wire; and

forming a second conductive wire, wherein the second interconnection region is electrically connected only to the second signal transmission region of the base plate by means of the second conductive wire.

14. The method of claim 12, further comprising:

forming a plurality of second pads on the first interconnection region, wherein a number of the first pads is greater than a number of the second pads; and an area of the first pad is less than an area of the second pad.

15. The method of claim 10, further comprising:

forming a second package structure, wherein the second package structure comprises a second solder ball and is electrically connected to the first solder ball by means of the second solder ball.

16. The method of claim 15, wherein a volume of the first solder ball is greater than a volume of the second solder ball.

17. The method of claim 15, wherein the molding compound has a first thickness in a direction perpendicular to the base plate; and

wherein the second package structure comprises a second molding compound; the second molding compound has a second thickness in the direction perpendicular to the base plate; and the first thickness is greater than or equal to the second thickness.