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DEVICE FOR PROCESSING TRANSMITTED DIGITAL VIDEO SIGNAL

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a device for processing video signals transmitted on a transmission line such as a magnetic recording/reproducing system in which erroneous codes are likely to be generated.

Related Background Art

In a conventional digital video signal reproducing apparatus such as a digital VTR as shown in Fig. 1, a rotary head 10 mounted on a rotary cylinder converts a magnetic signal recorded on a video tape into an electric signal which is amplified by an amplifier 12 and converted into a digital data by a data detection circuit 14 such as a comparator. The output data from the data detection circuit 14 contains errors in some cases. The output data is temporarily written in a memory 16 so that an error correction circuit 18 corrects errors while referring to error correction codes (to be described later) added when the data was recorded. Specifically, the error correction circuit 18 reads the data in the memory 16 to correct errors therein, and writes the corrected data again in the memory 16. The corrected data is read from the memory 16 and converted into an analog signals by a D/A converter 20 to be sent to a video apparatus (not shown) from a video output terminal 22.

In a digital recording system for recording a video signal in the form of a digital signal in a recording medium, error correction technique is generally used whereby one frame video data is divided into blocks each having a predetermined number of data, and an error correction code is added to each block when the data is recorded, to thereby correct errors at the time of recording/reproducing. In the reproducing operation, a predetermined number of errors generated at the time of recording/reproducing can be corrected by using error correction codes. Fig. 2 shows an example of a block format. In this format, "Sync" is a code representative of the top of a block. "ID" is a code representative of the frame area of each block or symbol. "CRCC (Cyclic Redundancy Check Code)" is an error detection correction code for ID. "Data" represents data in a block, and "P" is a parity for the above-described error correction code.

The data in each block is reproduced from a magnetic tape, and written in a frame memory at an area corresponding to its ID to them restore the original image.

Consider now that after recording a TV program in a video tape, another TV program is recorded in the remaining area of the video tape. Conventionally, the other TV program starts to be recorded regardless of the alignment of recording tracks, so that as shown in Fig. 3, the other program overwrites the previous program at the intersection area of track patterns. Accordingly, the width of the previous track becomes narrow at the intersection area so that data reproduction from the narrow track becomes difficult, resulting in an increased error rate of reproduced signals and in flickers in a reproduced image.

Further, a conventional video signal reproducing apparatus of such digital recording type has a problem that the quality of a reproduced image is considerably degraded during a reproducing operation other than a normal reproducing operation. For example, during a high speed search reproducing operation, the envelop level of an output from a reproducing head becomes very small periodically as shown in Fig. 4A to that the reproduced codes at such portion have a lower reliability and higher possibility of errors.

Also during the normal reproducing operation, if large foreign matters or dusts are maintained fixed to a reproducing head over several lines, disturbed images cannot be compensated even with a drop-out compensation circuit, resulting in large flickers in the reproduced image.

The above problems are commonly associated with an apparatus which transmits a digital video signal via a transmission line such as a magnetic recording/reproducing line having a high error occurrence possibility.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to solve the above problems under such circumstances.

It is another object of the present invention to provide a video signal processing device capable of suppressing flickers in a reproduced image even if video data is destructed during transmission.

According to an embodiment of the present invention which solves the above problems, there is provided a device for processing a digital code train including a video signal on a transmission line, comprising means for detecting a code error of said digital code train; a memory capable of writing

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said digital code train; and memory controlling means for controlling the writing of said digital code train into said memory in accordance with an output from said error detecting means.

The above and other objects and advantages of the present invention will become apparent from the following detailed description of embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing the structure of a conventional digital video signal reproducing apparatus;

Fig. 2 shows an example of a block format of video data recorded in a recording medium;

Fig. 3 shows an example of record patterns of video signals on a magnetic tape;

Figs. 4A to 4D are timing charts for explaining the video signal reproducing operations according to a prior art and embodiments of this invention;

Fig. 5 is a block diagram showing the structure of a digital video signal reproducing apparatus according to an embodiment of this invention;

Fig. 6 is a block diagram showing the structure of a digital video signal reproducing apparatus according to another embodiment of this invention; and

Fig. 7 is a block diagram showing the structure of a digital video signal reproducing apparatus according to a still further embodiment of this invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The embodiments of the present invention will be described with reference to the accompanying drawings.

Fig. 5 is a block diagram showing the structure of an embodiment of this invention. A rotary head 30 converts a magnetic signal on a video tape (not shown) into an electric signal which is amplified by an amplifier 32. Similar to the data detection circuit 14, a data detection circuit 34 converts an output from the amplifier 32 into a digital signal which is written in a memory 36.

Similar to the error correction circuit 18, an error correction circuit 38 corrects errors of the video data stored in the memory 36 while referring to error correction codes. In a digital VTR, one frame video data is divided into blocks each having a plurality of pixels, and the one frame video data has been subjected to various processings such as coding and error-correction-coding. The error correction circuit 38 not only corrects error but also outputs a check result signal 39 of an error check/correction parity for each block. The check result may by a "0" output for a block without error and a "1" output for a block with error. A counter 40 counts the check result signal 39 for each frame. Namely, the counter 40 outputs the number of error blocks per one frame. A comparator 42 compares an output from the counter 40 with a present value REF. If the number of blocks is the present value or more, a "1" signal is outputted, whereas if it is less than the present value REF, a "0" signal is outputted.

The data error-corrected by the error correction circuit 38 and stored in the memory 36 is read out therefrom and supplied to a frame memory 44. As will be understood from the later description, the video data one frame before has been stored in the frame memory 44. Therefore, if the comparator 42 outputs "1", the write operation into the frame memory 44 is stpopped for one frame, and only the read operation is allowed. In other words, video signals of the same frame are sequentially read from the frame memory 44 which is held in a freeze state. As a result, the frame memory 44 is inhibited to be renewed by the data stored in the memory 36. On the other hand, if the comparator 42 outputs "0", both the read and write operations for the frame memory 44 are permitted. Therefore, the frame memory 44 is renewed by the data stored in the memory 36.

The video data read from the frame memory 44 is converted into analog data by a D/A converter 46 and outputted to a video apparatus (not shown) via a video output terminal 48.

The operation of this embodiment will be described taking as an example the case as shown in Fig. 3. One frame video data is recorded respectively on tracks 50 and 51, tracks 52 and 53, and tracks 54 and 55. Although a frame image with less error can be reproduced from tracks 50 and 51, a reproduced image from tracks 52 and 53 has a number of errors because about half of the data on track 53 is destructed by track 54. According to this embodiment, assuming that the present value REF of the comparator 42 is set to one fourth the number of blocks constituting one frame, the frame memory 44 is held in a freeze state for inhibiting the data write operation into the memory 44 if the data corresponding to one fourth the frame is destructed. A reproduced image with less error at one frame before is outputted instead of the present frame.

Fig. 6 is a block diagram showing the structure of another embodiment of this invention. In this embodiment, in place of the counter 40 and comparator 42, there are provided an analog integrator 60 and a comparator 62 having an input/output hysteresis characteristic. Specifically, the ckeck result signal 39 from the error correction circuit 38 is

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integrated by the analog integrator 60, and the integrated signal is supplied to the comparator 62 by which the output of the integrator is compared with a threshold level having the hysteresis characteristic. The comparator 62 changes its output from "0" to "1" when an output of the integrator 60 exceeds a predetermined level Vth 1, and changes its output from "1" to "0" when the output lowers a predetermined level Vth 2 lower than Vth 1. An output of the comparator 62 controls the data write into the frame memory 44 in units of frame, in a similar manner to the comparator 42 shown in Fig. 5.

The embodiment shown in Fig. 6 can achieve the desired object with a relatively simple circuit arrangement.

As readily understood from the foregoing description, with the embodiments shown in Figs. 5 and 6, even if a number of video data are destructed, flickers in an image can be suppressed to thus allow a reproduced image of less flicker.

Fig. 7 is a block diagram showing the structure of a still further embodiment of this invention. Reference numeral 110 represents a magnetic tape on which a digital video signal is recorded, 112 a magnetic head, 114 an amplifier, 116 a reproduction circuit for converting an output (analog signal) from the amplifier 114 into a digital data signal, and 118 a Sync detection circuit for detecting a Sync code indicating the head of a block. A serial to parallel (S/P) converter 120 converts a serial data outputted from the reproduction circuit 116 into a parallel data of 8 or 4 bits. A timing generator 122 generates a predetermined timing signal in accordance with a Sync code detected by the Sync detection circuit 118.

An ID register 124 stores and ID within a reproduced block. An error decision circuit 26 decides in accordance with a CRCC added to the ID whether or not an error is present, and outputs a flag IDG if there is no error. A symbol counter 128 has a symbol data of ID as its initial value, and counts a data symbol of 8 or 4 bits. A block counter 30 uses as its initial value a block data of ID, and counts the number of blocks. An AND gate 132 controls the count of the counters 128 and 130 by using an output (IDG) from the error decision circuit 126. A comparator 136 compares an output from an analog low-pase filter (LPF) 134 with a predetermined threshold value. A system control circuit 138 controls the entirety of the circuit during a normal reproduction operation, a search operation and the like. A switch 140 is controlled to open or close by the system control circuit 138. A frame memory 142 is supplied with a write enable (WE) signal from an AND gate 144. The count of the symbol counter 128 is applied to the frame memory 142 as its lower address, and the count of the block memory 130 is supplies as the upper address.

The operation of the above embodiment will be described taking a search mode as an example. An output of the magnetic head 112 is amplified by the amplifier 114 and converted into a digital data by the reproduction circuit 116. The output from the reproduction circuit 116 is a code train of the block structure as shown in Fig. 2. The Sync detection circuit 118 detects the top code of the block. In accordance with an output from the Sync detection circuit 118, the timing generator 122 generates a fetch timing signal for the ID register 124, a reset timing signal for the counters 128 and 130, and other timing signals.

An output data from the reproduction circuit 116 is converted into a parallel data by the S/P convereter 120. The ID data is sotred in the ID register 124, and is loaded as the initial value into the symbol counter 128 and block counter 130. Under the state that the reproduced output level of the magnetic head 112 is sufficiently high, there is scarcely any error in the ID information so that the error decision circuit 126 outputs the flag IDG in a stable manner. Accordingly, the AND gate 132 supplies the output from the timing generation circuit 122 to the counters 128 and 130 in a stable manner. The counts of the counters 128 and 130 are supplied as the lower and upper addresses to the frame memory 142 so that the video data outputted from the S/P converter 120 is written in the frame memory 142 at the designated address.

With the above operation, the block video data reproduced from the magnetic tape is written in the frame memory 142. Next, there will be described the operation when the reproduced output level of the magnetic head 112 has lowered. In this case, there are many errors in the reproduced data. The error decision circuit 126 detects error in accordance with the CRCC contained in the ID information in the ID register 124. If there are errors, the circuit tends to output less the flag IDG as shown in Fig. 4B. More in particular, while the envelope level of a reproduced output from the magnetic head 112 is large, the flag IDG is generated in a stable manner. However, while the envelope level of a reduced output is small, the flag IDG is scarcely generated, and during the intermediate region, the flag IDG is generated in an unstable manner. The output (Fig. 4B) from the error decision circuit 126 has the waveform as shown in Fig. 4C after passing through LPF 134, and has the waveform as shown in Fig. 4D after passing through the comparator 136. The output from the comparator 136 operates as the signal for judging if there is an error in the ID information.

The switch 140 is closed if LPF 134 and comparator 136 are used, i.e., if a specific reproduction operation is to be used. The output from the com-

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parator 136 is supplied via the switch 140 to the AND gate 144. The AND gate 144 is closed if an error is always or occasionally present in the ID information, to thereby prohibit the application of the write enable signal to the frame memory 142. As a result, the reproduced data, i.e., image data assumed to contain many error, is not written in the frame memory 142 and a relatively good search image can be obtained.

As readily understood from the foregoing description, according to the embodiment shown in Fig. 7, it is possible to obtain by using a very simple structure a signal which judges an occurrence of error in the reproduced data. This signal is used for controlling the write operation of the image memory, to thereby obtain a good reproduced image.

A digital VTR has been used as an example in the above embodiment. This embodiment is applicable not only to a tape type recording medium, but also other recording medium such as an optical disk, magnetooptical disk and the like whereby when the data becomes difficult to be read from such a recording medium because of scratches or the like, the write operation of video signals into the memory is prohibited to suppress flickers in a reproduced image output. Further, if the embodiment is applied to a receiver in a system wherein a video signal is transmitted via a transmission path such as a radio transmission, wire transmission or the like, flickers in a reproduced image due to various interference waves can be avoided. Namely, the invention is advantageously applicable to a system wherein a moving image is recorded digitally or transmitted, and particularly applicable to a system which has a possibility of data destruction by some reason.

Claims

1. A device for processing a digital code train including a video signal on a transmission line, comprising

(a) means for detecting a code error of said digital code train;

(b) a memory capable of being written said digital code train; and

(c) memory controlling means for controlling the writing of said digital code train into said memory in accordance with an output from said error detecting means.

2. A device according to claim 1, wherein said code train comprises a number of data blocks each having a video signal and an error detection/correction code, and
said error detecting means detects a presence of a code error in each data block by using said error detection/correction code, and outputs a flag in accordance with the detection result.

3. A device according to Claim 2, wherein each of said number of data blocks includes an error correction parity word, and
said error detecting means has a function to correct a code error within said data block by using said parity word, and outputs said flag in response to an occurrence of a data block which cannot be corrected.

4. A device according to Claim 3, wherein
said memory is constructed such that said digital code train with at least some code thereof having been corrected by said error detecting means.

5. A device according to Claim 2, wherin
said memory controlling means includes a flag processing circuit for detecting an occurrence frequency of said flag, and the write operation of said digital code train into said memory is controlled by an output from said flag processing circuit.

6. A device according to claim 5, wherein
said flag processing circuit detects the occurrence frequency of said flag within a predetermined period.

7. A device according to Claim 6, wherein
said memory controlling means controls the write operation of said digital code train into said memory in units of said predetermined period.

8. A device according to Claim 7, wherein
said predetermined period corresponds to the one frame period of said video signal.

9. A device according to Claim 6, wherein
said flag processing circuit comprises a counter for counting said flag generated during said predetermined period, and a comparator for comparing said count value by said counter with a predetermined value.

10. A device according to Claim 5, wherein
said flag is a binary signal, and said flag processing circuit includes a circuit for eliminating the high frequency components of said binary signal.

11. A device according to Claim 10, wherein
said eliminating circuit comprises a low-pass filter to which said binary signal is inputted, and a comparator for comparing an output from said low-pass filter with a predetermined value.

12. A device according to Claim 11, wherein
an output from said comparator changes from a first value to a second value when an output from said low-pass filter exceeds a first predetermined level, and from said second value to said first value when an output from said low-pass filter becomes smaller than a second predetermined level, said first predetermined level being higher than said second predetermined level.

13 A device according to Claim 2, wherin
each of said number of data blocks includes an allocation data representative of the allocation of

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parator 136 is supplied via the switch 140 to the AND gate 144. The AND gate 144 is closed if an error is always or occasionally present in the ID information, to thereby prohibit the application of the write enable signal to the frame memory 142. As a result, the reproduced data, i.e., image data assumed to contain many error, is not written in the frame memory 142 and a relatively good search image can be obtained.

As readily understood from the foregoing description, according to the embodiment shown in Fig. 7, it is possible to obtain by using a very simple structure a signal which judges an occurrence of error in the reproduced data. This signal is used for controlling the write operation of the image memory, to thereby obtain a good reproduced image.

A digital VTR has been used as an example in the above embodiment. This embodiment is applicable not only to a tape type recording medium, but also other recording medium such as an optical disk, magnetooptical disk and the like whereby when the data becomes difficult to be read from such a recording medium because of scratches or the like, the write operation of video signals into the memory is prohibited to suppress flickers in a reproduced image output. Further, if the embodiment is applied to a receiver in a system wherein a video signal is transmitted via a transmission path such as a radio transmission, wire transmission or the like, flickers in a reproduced image due to various interference waves can be avoided. Namely, the invention is advantageously applicable to a system wherein a moving image is recorded digitally or transmitted, and particularly applicable to a system which has a possibility of data destruction by some reason.

Claims

1. A device for processing a digital code train including a video signal on a transmission line, comprising

(a) means for detecting a code error of said digital code train;

(b) a memory capable of being written said digital code train; and

(c) memory controlling means for controlling the writing of said digital code train into said memory in accordance with an output from said error detecting means.

2. A device according to claim 1, wherein said code train comprises a number of data blocks each having a video signal and an error detection/correction code, and
said error detecting means detects a presence of a code error in each data block by using said error detection/correction code, and outputs a flag in accordance with the detection result.

3. A device according to Claim 2, wherein each of said number of data blocks includes an error correction parity word, and
said error detecting means has a function to correct a code error within said data block by using said parity word, and outputs said flag in response to an occurrence of a data block which cannot be corrected.

4. A device according to Claim 3, wherein
said memory is constructed such that said digital code train with at least some code thereof having been corrected by said error detecting means.

5. A device according to Claim 2, wherin
said memory controlling means includes a flag processing circuit for detecting an occurrence frequency of said flag, and the write operation of said digital code train into said memory is controlled by an output from said flag processing circuit.

6. A device according to claim 5, wherein
said flag processing circuit detects the occurrence frequency of said flag within a predetermined period.

7. A device according to Claim 6, wherein
said memory controlling means controls the write operation of said digital code train into said memory in units of said predetermined period.

8. A device according to Claim 7, wherein
said predetermined period corresponds to the one frame period of said video signal.

9. A device according to Claim 6, wherein
said flag processing circuit comprises a counter for counting said flag generated during said predetermined period, and a comparator for comparing said count value by said counter with a predetermined value.

10. A device according to Claim 5, wherein
said flag is a binary signal, and said flag processing circuit includes a circuit for eliminating the high frequency components of said binary signal.

11. A device according to Claim 10, wherein
said eliminating circuit comprises a low-pass filter to which said binary signal is inputted, and a comparator for comparing an output from said low-pass filter with a predetermined value.

12. A device according to Claim 11, wherein
an output from said comparator changes from a first value to a second value when an output from said low-pass filter exceeds a first predetermined level, and from said second value to said first value when an output from said low-pass filter becomes smaller than a second predetermined level, said first predetermined level being higher than said second predetermined level.

13 A device according to Claim 2, wherin
each of said number of data blocks includes an allocation data representative of the allocation of

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said video signal of said data block within a frame screen, and said memory controlling means writes said each data block in said memory at an address corresponding to said allocation data.

14. A device according to Claim 2, wherein each of said number of data blocks includes an error detection code capable of detecting an error of only said allocation data, and said error detecting means outputs said flag in accordance with an error detection result of said allocation data by said error detection code.

15. A device for processing a digital code train on a transmission path including a video signal, comprising:

(a) error detecting means for detecting a code error of said digital code train;

(b) a memory capable of being written said digital code train; and

(c) mode changing means for changing said device between first and second modes in accordance with an output from said error detecting means, said first mode controlling the write operation of said digital code train into said memory, and said second mode writing said digital code train into said memory irrespective of an output from said error detecing means.

16. A device according to Claim 15, wherein said code train comprises a number of data blocks each including a video signal and an error detection/correction code, and
said error detecting means detects if there is a code error in each data block by using said error detection/correction code, and outputs a flag in accordance with the detection result.

17. A device according to claim 16, wherein said memory controlling means includes a flag processing circuit for detecting an occurrence frequency of said flag, and the write operation of said digital code train into said memory is controlled in accordance with an output from said flag processing circuit.

18. A device according to Claim 17, wherein said flag processing circuit detects an occurrence frequency of said flag within one frame of said video signal, and said memory controlling means controls the write operation of said digital code train into said memory in units of said one frame of said video signal.

19. A device according to Claim 17, wherein said flag is a binary signal, and said flag processing circuit includes a circuit for elliminating the high frequency components of said binary signal.

20. A method or apparatus for processing a digital data train representing a video signal, in which errors in the digital data train are detected, and at least a portion of the digital data train which portion represents a video signal is selectively either written into a memory means or not in accordance with the said detected errors.

21. A device for processing a digital code train including a video signal on a transmission line, wherein the write operation of the digital code train into a memory is controlled in accordance with an output from an error detection circuit for detecting a code error of the digital code train, thereby obtaining a good image even if some code of the digital code train is destroyed.

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FIG. 1

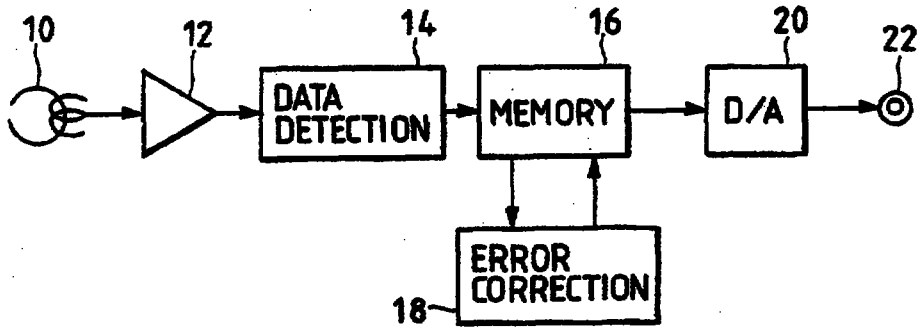
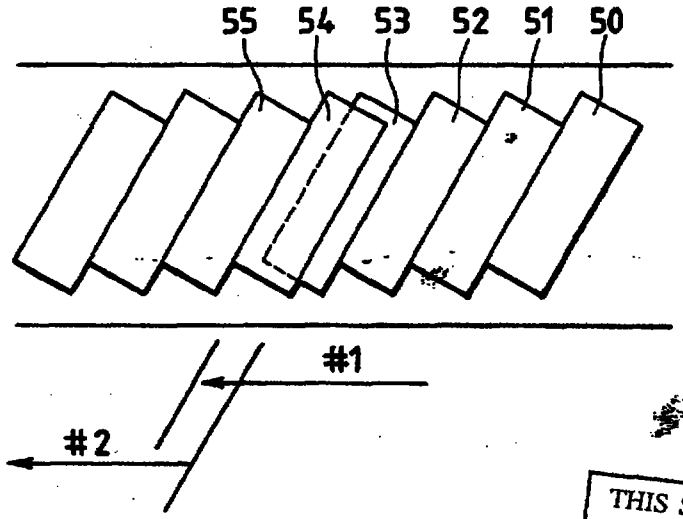


FIG. 2



FIG. 3



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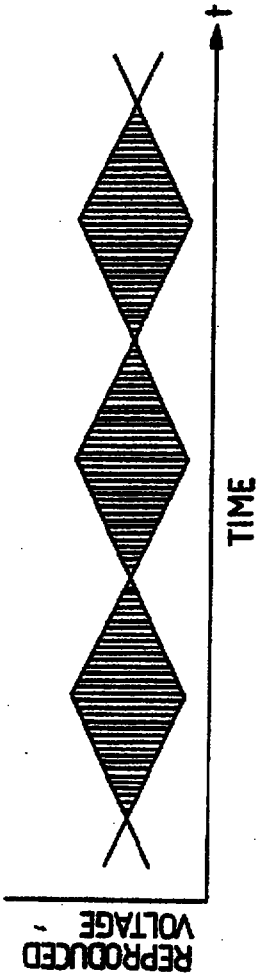


FIG. 4A

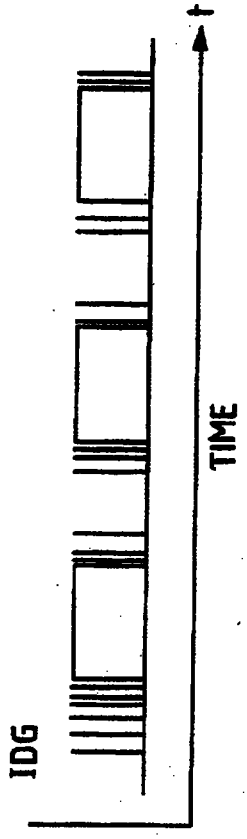


FIG. 4B

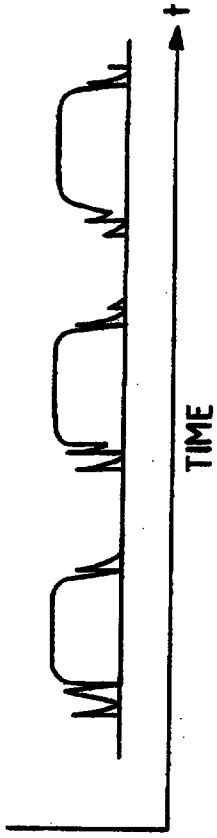


FIG. 4C

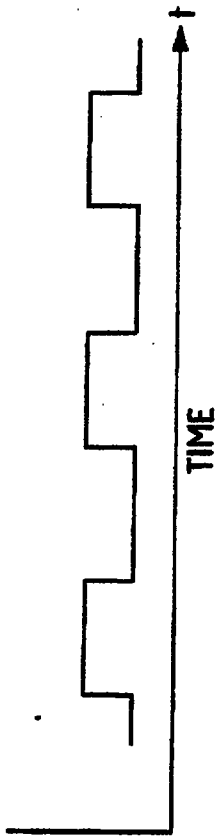


FIG. 4D

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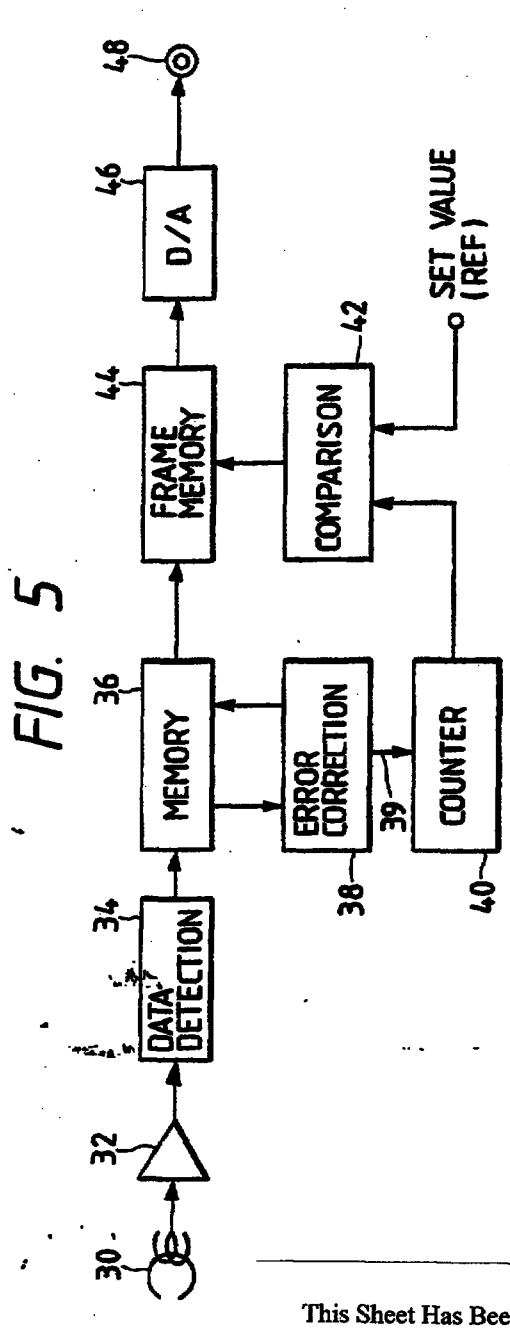


FIG. 5

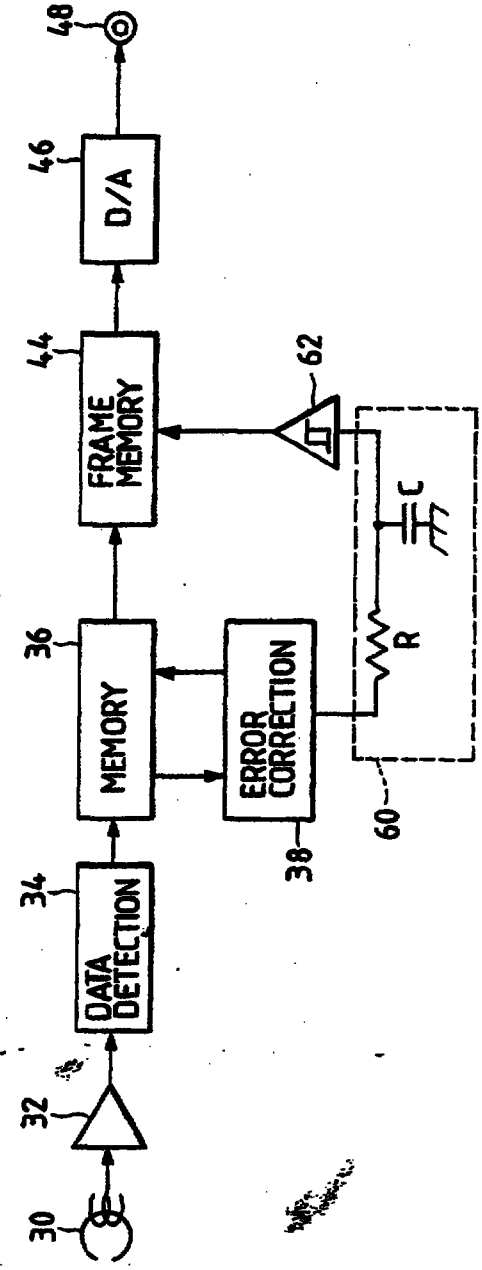


FIG. 6

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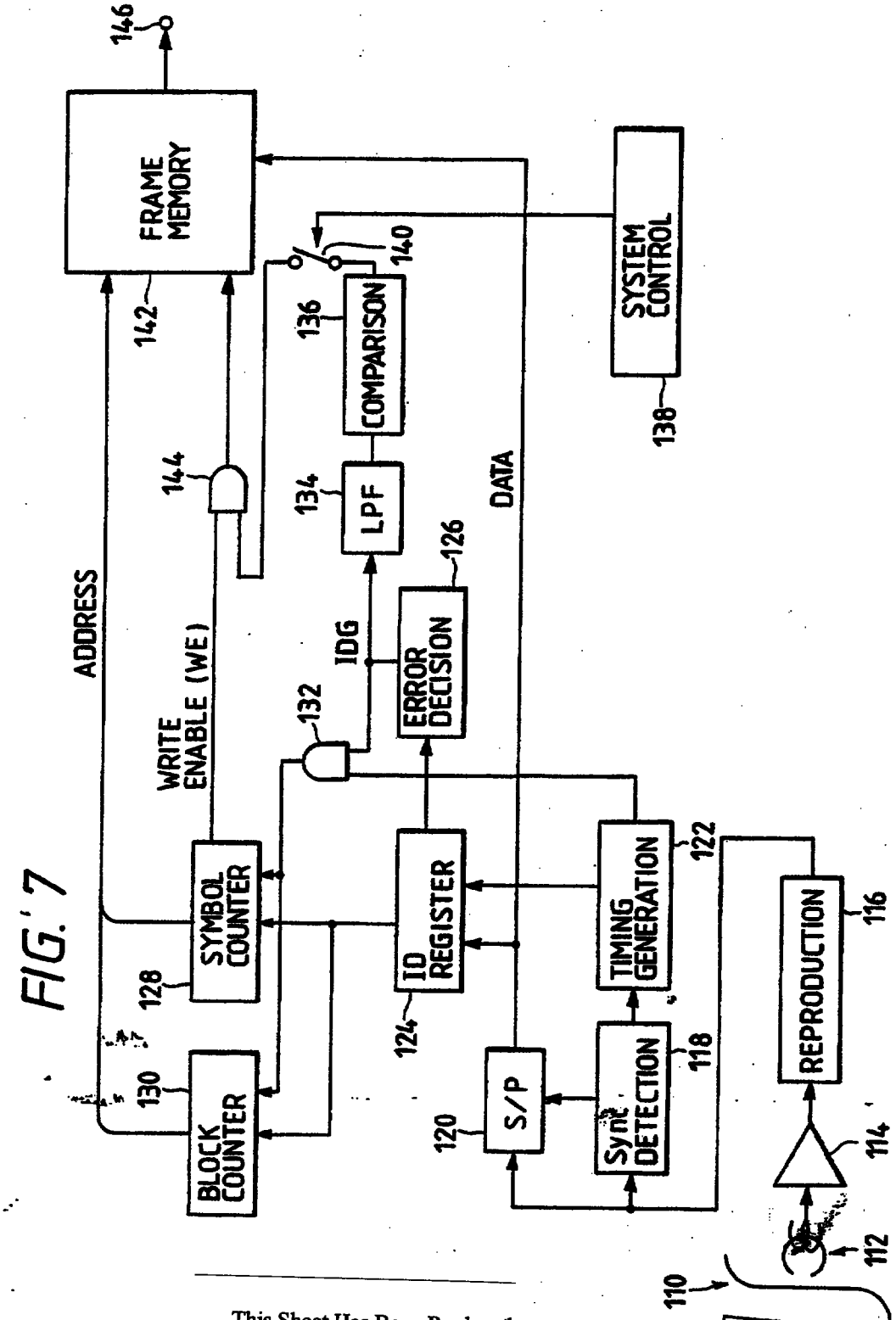


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DEVICE FOR PROCESSING TRANSMITTED DIGITAL VIDEO SIGNAL

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a device for processing video signals transmitted on a transmission line such as a magnetic recording/reproducing system in which erroneous codes are likely to be generated.

Related Background Art

In a conventional digital video signal reproducing apparatus such as a digital VTR as shown in Fig. 1, a rotary head 10 mounted on a rotary cylinder converts a magnetic signal recorded on a video tape into an electric signal which is amplified by an amplifier 12 and converted into a digital data by a data detection circuit 14 such as a comparator. The output data from the data detection circuit 14 contains errors in some cases. The output data is temporarily written in a memory 16 so that an error correction circuit 18 corrects errors while referring to error correction codes (to be described later) added when the data was recorded. Specifically, the error correction circuit 18 reads the data in the memory 16 to correct errors therein, and writes the corrected data again in the memory 16. The corrected data is read from the memory 16 and converted into an analog signals by a D/A converter 20 to be sent to a video apparatus (not shown) from a video output terminal 22.

In a digital recording system for recording a

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video signal in the form of a digital signal in a recording medium, error correction technique is generally used whereby one frame video data is divided into blocks each having a predetermined number of data, and an error correction code is added to each block when the data is recorded, to thereby correct errors at the time of recording/reproducing. In the reproducing operation, a predetermined number of errors generated at the time of recording/reproducing can be corrected by using error correction codes. Fig. 2 shows an example of a block format. In this format, "Sync" is a code representative of the top of a block. "ID" is a code representative of the frame area of each block or symbol. "CRCC (Cyclic Redundancy Check Code)" is an error detection correction code for ID. "Data" represents data in a block, and "P" is a parity for the above-described error correction code.

The data in each block is reproduced from a magnetic tape, and written in a frame memory at an area corresponding to its ID to them restore the original image.

Consider now that after recording a TV program in a video tape, another TV program is recorded in the remaining area of the video tape. Conventionally, the other TV program starts to be recorded regardless of the alignment of recording tracks, so that as shown in Fig. 3, the other program overwrites the previous program at the intersection area of track patterns. Accordingly,

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the width of the previous track becomes narrow at the intersection area so that data reproduction from the narrow track becomes difficult, resulting in an increased error rate of reproduced signals and in flickers in a reproduced image.

Further, a conventional video signal reproducing apparatus of such digital recording type has a problem that the quality of a reproduced image is considerably degraded during a reproducing operation other than a normal reproducing operation. For example, during a high speed search reproducing operation, the envelop level of an output from a reproducing head becomes very small periodically as shown in Fig. 4A to that the reproduced codes at such portion have a lower reliability and higher possibility of errors.

Also during the normal reproducing operation, if large foreign matters or dusts are maintained fixed to a reproducing head over several lines, disturbed images cannot be compensated even with a drop-out compensation circuit, resulting in large flickers in the reproduced image.

The above problems are commonly associated with an apparatus which transmits a digital video signal via a transmission line such as a magnetic recording/ reproducing line having a high error occurrence possibility.

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SUMMARY OF THE INVENTION

It is therefore an object of the present invention to solve the above problems under such circumstances.

It is another object of the present invention to provide a video signal processing device capable of suppressing flickers in a reproduced image even if video data is destructed during transmission.

According to an embodiment of the present invention which solves the above problems, there is provided a device for processing a digital code train including a video signal on a transmission line, comprising means for detecting a code error of said digital code train; a memory capable of writing said digital code train; and memory controlling means for controlling the writing of said digital code train into said memory in accordance with an output from said error detecting means.

The above and other objects and advantages of the present invention will become apparent from the following detailed description of embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing the structure of a conventional digital video signal reproducing apparatus;

Fig. 2 shows an example of a block format of video data recorded in a recording medium;

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Fig. 3 shows an example of record patterns of video signals on a magnetic tape;

Figs. 4A to 4D are timing charts for explaining the video signal reproducing operations according to a prior art and embodiments of this invention;

Fig. 5 is a block diagram showing the structure of a digital video signal reproducing apparatus according to an embodiment of this invention;

Fig. 6 is a block diagram showing the structure of a digital video signal reproducing apparatus according to another embodiment of this invention; and

Fig. 7 is a block diagram showing the structure of a digital video signal reproducing apparatus according to a still further embodiment of this invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The embodiments of the present invention will be described with reference to the accompanying drawings.

Fig. 5 is a block diagram showing the structure of an embodiment of this invention. A rotary head 30 converts a magnetic signal on a video tape (not shown) into an electric signal which is amplified by an amplifier 32. Similar to the data detection circuit 14, a data detection circuit 34 converts an output from the amplifier 32 into a digital signal which is written in a memory 36.

Similar to the error correction circuit 18, an error correction circuit 38 corrects errors of the video

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data stored in the memory 36 while referring to error correction codes. In a digital VTR, one frame video data is divided into blocks each having a plurality of pixels, and the one frame video data has been subjected to various processings such as coding and error-correction-coding. The error correction circuit 38 not only corrects error but also outputs a check result signal 39 of an error check/correction parity for each block. The check result may by a "0" output for a block without error and a "1" output for a block with error. A counter 40 counts the check result signal 39 for each frame. Namely, the counter 40 outputs the number of error blocks per one frame. A comparator 42 compares an output from the counter 40 with a present value REF. If the number of blocks is the present value or more, a "1" signal is outputted, whereas if it is less than the present value REF, a "0" signal is outputted.

The data error-corrected by the error correction circuit 38 and stored in the memory 36 is read out therefrom and supplied to a frame memory 44. As will be understood from the later description, the video data one frame before has been stored in the frame memory 44. Therefore, if the comparator 42 outputs "1", the write operation into the frame memory 44 is stpopped for one frame, and only the read operation is allowed. In other words, video signals of the same frame are sequentially read from the frame memory 44 which is held

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in a freeze state. As a result, the frame memory 44 is inhibited to be renewed by the data stored in the memory 36. On the other hand, if the comparator 42 outputs "0", both the read and write operations for the frame memory 44 are permitted. Therefore, the frame memory 44 is renewed by the data stored in the memory 36.

The video data read from the frame memory 44 is converted into analog data by a D/A converter 46 and outputted to a video apparatus (not shown) via a video output terminal 48.

The operation of this embodiment will be described taking as an example the case as shown in Fig. 3. One frame video data is recorded respectively on tracks 50 and 51, tracks 52 and 53, and tracks 54 and 55. Although a frame image with less error can be reproduced from tracks 50 and 51, a reproduced image from tracks 52 and 53 has a number of errors because about half of the data on track 53 is destructed by track 54. According to this embodiment, assuming that the present value REF of the comparator 42 is set to one fourth the number of blocks constituting one frame, the frame memory 44 is held in a freeze state for inhibiting the data write operation into the memory 44 if the data corresponding to one fourth the frame is destructed. A reproduced image with less error at one frame before is outputted instead of the present frame.

Fig. 6 is a block diagram showing the structure

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of another embodiment of this invention. In this embodiment, in place of the counter 40 and comparator 42, there are provided an analog integrator 60 and a comparator 62 having an input/output hysteresis characteristic. Specifically, the ckeck result signal 39 from the error correction circuit 38 is integrated by the analog integrator 60, and the integrated signal is supplied to the comparator 62 by which the output of the integrator 60 is compared with a threshold level having the hysteresis characteristic. The comparator 62 changes its output from "0" to "1" when an output of the integrator 60 exceeds a predetermined level Vth 1, and changes its output from "1" to "0" when the output lowers a predetermined level Vth 2 lower than Vth 1. An output of the comparator 62 controls the data write into the frame memory 44 in units of frame, in a similar manner to the comparator 42 shown in Fig. 5.

The embodiment shown in Fig. 6 can achieve the desired object with a relatively simple circuit arrangement.

As readily understood from the foregoing description, with the embodiments shown in Figs. 5 and 6, even if a number of video data are destructed, flickers in an image can be suppressed to thus allow a reproduced image of less flicker.

Fig. 7 is a block diagram showing the structure of a still further embodiment of this invention. Reference numeral 110 represents a magnetic tape on which

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a digital video signal is recorded, 112 a magnetic head, 114 an amplifier, 116 a reproduction circuit for converting an output (analog signal) from the amplifier 114 into a digital data signal, and 118 a Sync detection circuit for detecting a Sync code indicating the head of a block. A serial to parallel (S/P) converter 120 converts a serial data outputted from the reproduction circuit 116 into a parallel data of 8 or 4 bits. A timing generator 122 generates a predetermined timing signal in accordance with a Sync code detected by the Sync detection circuit 118.

An ID register 124 stores and ID within a reproduced block. An error decision circuit 26 decides in accordance with a CRCC added to the ID whether or not an error is present, and outputs a flag IDG if there is no error. A symbol counter 128 has a symbol data of ID as its initial value, and counts a data symbol of 8 or 4 bits. A block counter 30 uses as its initial value a block data of ID, and counts the number of blocks. An AND gate 132 controls the count of the counters 128 and 130 by using an output (IDG) from the error decision circuit 126. A comparator 136 compares an output from an analog low-pass filter (LPF) 134 with a predetermined threshold value. A system control circuit 138 controls the entirety of the circuit during a normal reproduction operation, a search operation and the like. A switch 140 is controlled to open or close by the system control

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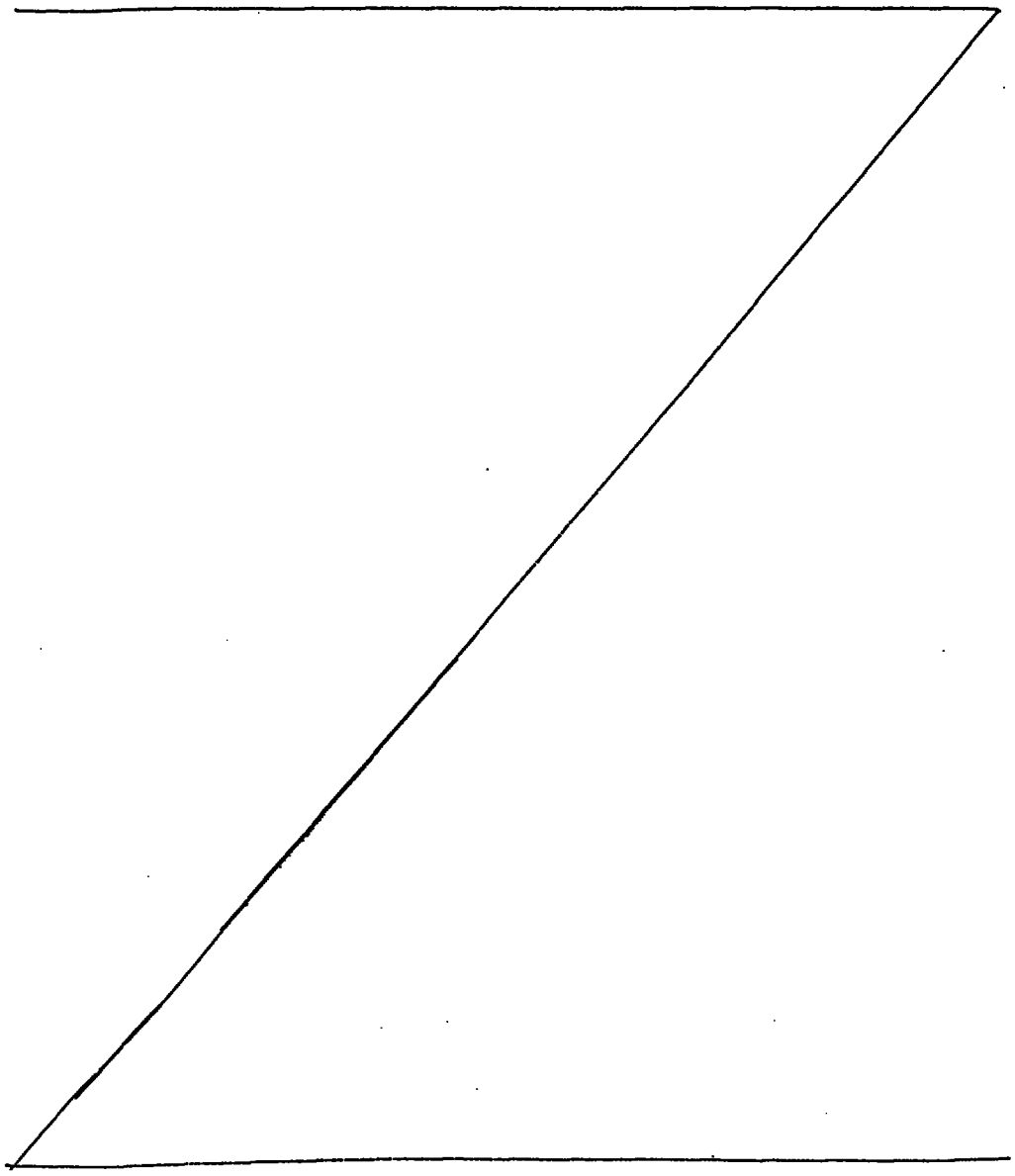
circuit 138. A frame memory 142 is supplied with a write enable (WE) signal from an AND gate 144. The count of the symbol counter 128 is applied to the frame memory 142 as its lower address, and the count of the block memory 130 is supplies as the upper address.

The operation of the above embodiment will be described taking a search mode as an example. An output of the magnetic head 112 is amplified by the amplifier 114 and converted into a digital data by the reproduction circuit 116. The output from the reproduction circuit 116 is a code train of the block structure as shown in Fig. 2. The Sync detection circuit 118 detects the top code of the block. In accordance with an output from the Sync detection circuit 118, the timing generator 122 generates a fetch timing signal for the ID register 124, a reset timing signal for the counters 128 and 130, and other timing signals.

An output data from the reproduction circuit 116 is converted into a parallel data by the S/P convereter 120. The ID data is sotred in the ID register 124, and is loaded as the initial value into the symbol counter 128 and block counter 130. Under the state that the reproduced output level of the magnetic head 112 is sufficiently high, there is scarcely any error in the ID information so that the error decision circuit 126 outputs the flag IDG in a stable manner. Accordingly, the AND gate 132 supplies the output from the timing generation circuit

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122 to the counters 128 and 130 in a stable manner. The counts of the counters 128 and 130 are supplied as the lower and upper addresses to the frame memory 142 so that the video data outputted from the S/P converter 120 is written in the frame memory 142 at the designated address.



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With the above operation, the block video data reproduced from the magnetic tape is written in the frame memory 142. Next, there will be described the operation when the reproduced output level of the magnetic head 112 has lowered. In this case, there are many errors in the reproduced data. The error decision circuit 126 detects error in accordance with the CRCC contained in the ID information in the ID register 124. If there are errors, the circuit tends to output less the flag IDG as shown in Fig. 4B. More in particular, while the envelope level of a reproduced output from the magnetic head 112 is large, the flag IDG is generated in a stable manner. However, while the envelope level of a reduced output is small, the flag IDG is scarcely generated, and during the intermediate region, the flag IDG is generated in an unstable manner. The output (Fig. 4B) from the error decision circuit 126 has the waveform as shown in Fig. 4C after passing through LPF 134, and has the waveform as shown in Fig. 4D after passing through the comparator 136. The output from the comparator 136 operates as the signal for judging if there is an error in the ID information.

The switch 140 is closed if LPF 134 and comparator 136 are used, i.e., if a specific reproduction operation is to be used. The output from the comparator 136 is supplied via the switch 140 to the AND gate 144. The AND gate 144 is closed if an error is always or

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occasionally present in the ID information, to thereby prohibit the application of the write enable signal to the frame memory 142. As a result, the reproduced data, i.e., image data assumed to contain many error, is not written in the frame memory 142 and a relatively good search image can be obtained.

As readily understood from the foregoing description, according to the embodiment shown in Fig. 7, it is possible to obtain by using a very simple structure a signal which judges an occurrence of error in the reproduced data. This signal is used for controlling the write operation of the image memory, to thereby obtain a good reproduced image.

A digital VTR has been used as an example in the above embodiment. This embodiment is applicable not only to a tape type recording medium, but also other recording medium such as an optical disk, magnetooptical disk and the like whereby when the data becomes difficult to be read from such a recording medium because of scratches or the like, the write operation of video signals into the memory is prohibited to suppress flickers in a reproduced image output. Further, if the embodiment is applied to a receiver in a system wherein a video signal is transmitted via a transmission path such as a radio transmission, wire transmission or the like, flickers in a reproduced image due to various interference waves can be avoided. Namely,

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the invention is advantageously applicable to a system wherein a moving image is recorded digitally or transmitted, and particularly applicable to a system which has a possibility of data destruction by some reason.

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WHAT IS CLAIMED IS:

1. A device for processing a digital code train including a video signal on a transmission line, comprising

(a) means for detecting a code error of said digital code train;

(b) a memory capable of being written said digital code train; and

(c) memory controlling means for controlling the writing of said digital code train into said memory in accordance with an output from said error detecting means.

2. A device according to claim 1, wherein

said code train comprises a number of data blocks each having a video signal and an error detection/correction code, and

said error detecting means detects a presence of a code error in each data block by using said error detection/correction code, and outputs a flag in accordance with the detection result.

3. A device according to Claim 2, wherein

each of said number of data blocks includes an error correction parity word, and

said error detecting means has a function to correct a code error within said data block by using said parity word, and outputs said flag in response

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to an occurrence of a data block which cannot be corrected.

4. A device according to Claim 3, wherein said memory is constructed such that said digital code train with at least some code thereof having been corrected by said error detecting means.

5. A device according to Claim 2, wherin said memory controlling means includes a flag processing circuit for detecting an occurrence frequency of said flag, and the write operation of said digital code train into said memory is controlled by an output from said flag processing circuit.

6. A device according to claim 5, wherein said flag processing circuit detects the occurrence frequency of said flag within a predetermined period.

7. A device according to Claim 6, wherein said memory controlling means controls the write operation of said digital code train into said memory in units of said predetermined period.

8. A device according to Claim 7, wherein said predetermined period corresponds to the one frame period of said video signal.

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9. A device according to Claim 6, wherein said flag processing circuit comprises a counter for counting said flag generated during said predetermined period, and a comparator for comparing said count value by said counter with a predetermined value.

10. A device according to Claim 5, wherein said flag is a binary signal, and said flag processing circuit includes a circuit for eliminating the high frequency components of said binary signal.

11. A device according to Claim 10, wherein said eliminating circuit comprises a low-pass filter to which said binary signal is inputted, and a comparator for comparing an output from said low-pass filter with a predetermined value.

12. A device according to Claim 11, wherein an output from said comparator changes from a first value to a second value when an output from said low-pass filter exceeds a first predetermined level, and from said second value to said first value when an output from said low-pass filter becomes smaller than a second predetermined level, said first predetermined level being higher than said second predetermined level.

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13. A device according to Claim 2, wherin each of said number of data blocks includes an allocation data representative of the allocation of said video signal of said data block within a frame screen, and said memory controlling means writes said each data block in said memory at an address corresponding to said allocation data.

14. A device according to Claim 2, wherein each of said number of data blocks includes an error detection code capable of detecting an error of only said allocation data, and said error detecting means outputs said flag in accordance with an error detection result of said allocation data by said error detection code.

15. A device for processing a digital code train on a transmission path including a video signal, comprising:

(a) error detecting means for detecting a code error of said digital code train;

(b) a memory capable of being written said digital code train; and

(c) mode changing means for changing said device between first and second modes in accordance with an output from said error detecting means, said first mode controlling the write operation of said digital code

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train into said memory, and said second mode writing said digital code train into said memory irrespective of an output from said error detecing means.

16. A device according to Claim 15, wherein said code train comprises a number of data blocks each including a video signal and an error detection/correction code, and

said error detecting means detects if there is a code error in each data block by using said error detection/correction code, and outputs a flag in accordance with the detection result.

17. A device according to claim 16, wherein said memory controlling means includes a flag processing circuit for detecting an occurrence frequency of said flag, and the write operation of said digital code train into said memory is controlled in accordance with an output from said flag processing circuit.

18. A device according to Claim 17, wherein said flag processing circuit detects an occurrence frequency of said flag within one frame of said video signal, and said memory controlling means controls the write operation of said digital code train into said memory in units of said one frame of said video signal.

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19. A device according to Claim 17, wherein said flag is a binary signal, and said flag processing circuit includes a circuit for eliminating the high frequency components of said binary signal.

20. A method or apparatus for processing a digital data train representing a video signal, in which errors in the digital data train are detected, and at least a portion of the digital data train which portion represents a video signal is selectively either written into a memory means or not in accordance with the said detected errors.

21. A device for processing a digital code train including a video signal on a transmission line, wherein the write operation of the digital code train into a memory is controlled in accordance with an output from an error detection circuit for detecting a code error of the digital code train, thereby obtaining a good image even if some code of the digital code train is destroyed.

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ABSTRACT:

DEVICE FOR PROCESSING TRANSMITTED DIGITAL VIDEO SIGNAL

A device for processing a digital code train including a video signal on a transmission line, wherein the write operation of the digital code train into a memory is controlled in accordance with an output from an error detection circuit for detecting a code error of the digital code train, thereby obtaining a good image even if some code of the digital code train is destroyed.

FIGURE 5

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FIG. 1

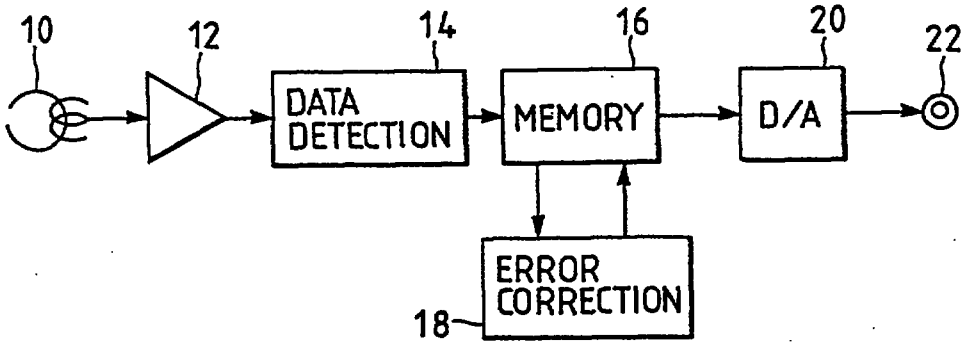
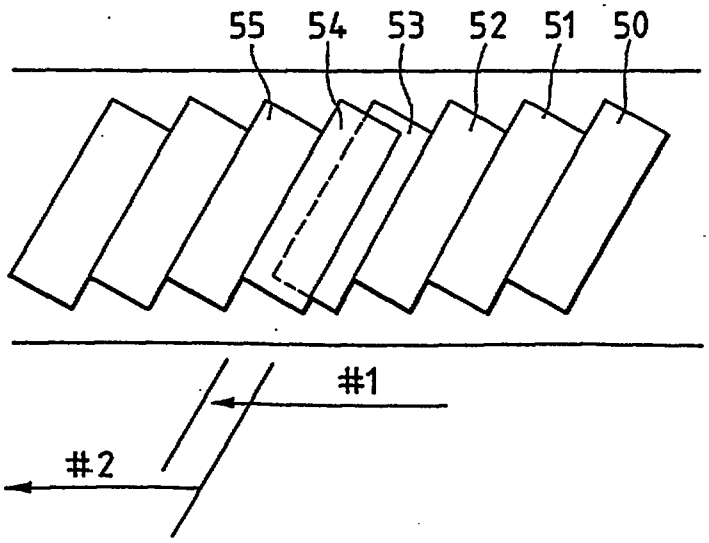


FIG. 2



FIG. 3



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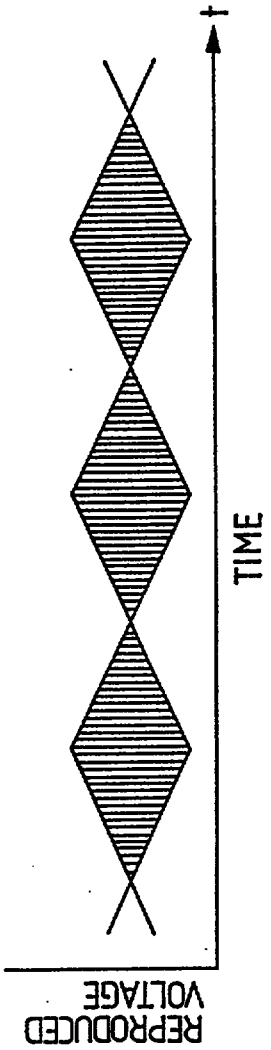


FIG. 4A

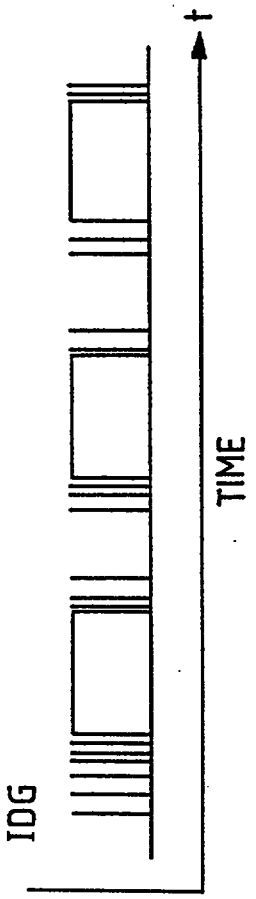


FIG. 4B

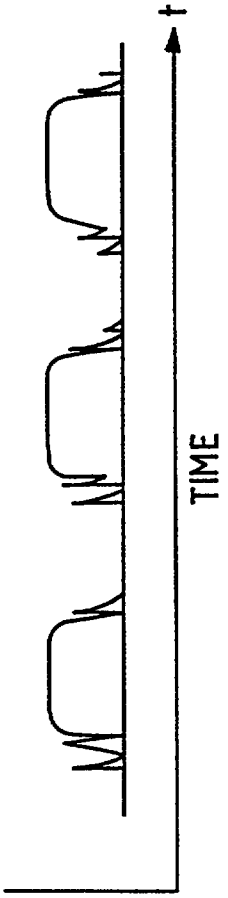


FIG. 4C

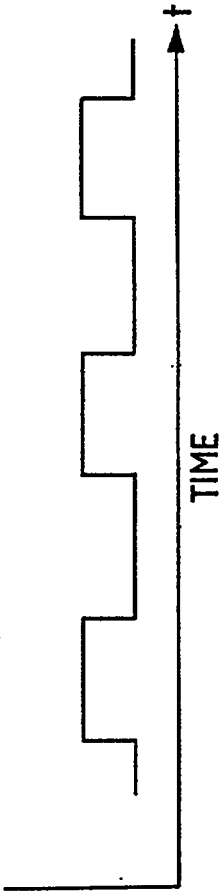


FIG. 4D

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FIG. 5

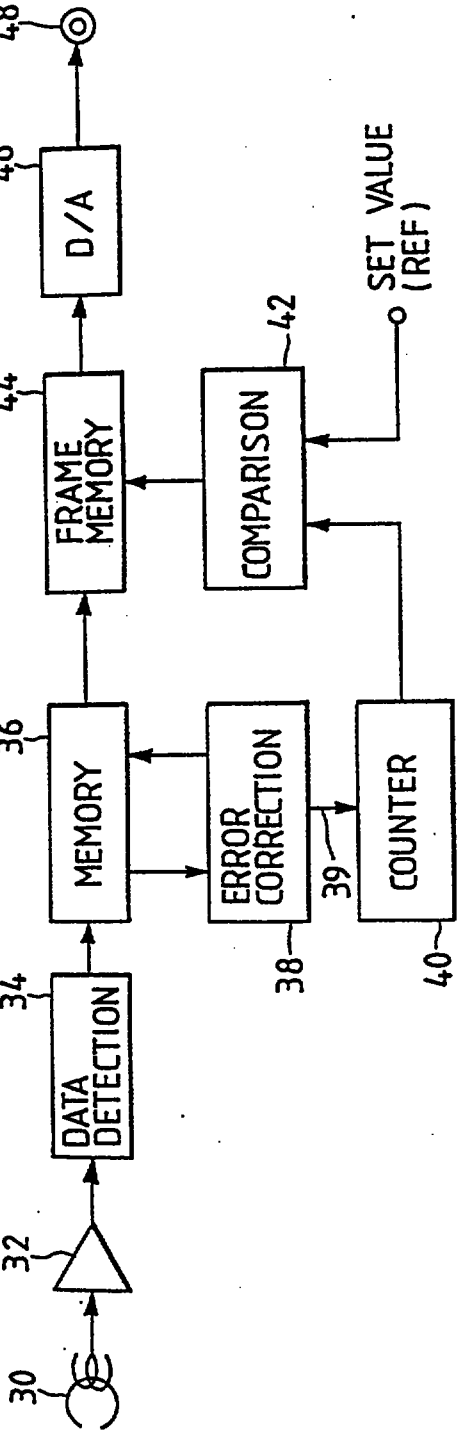
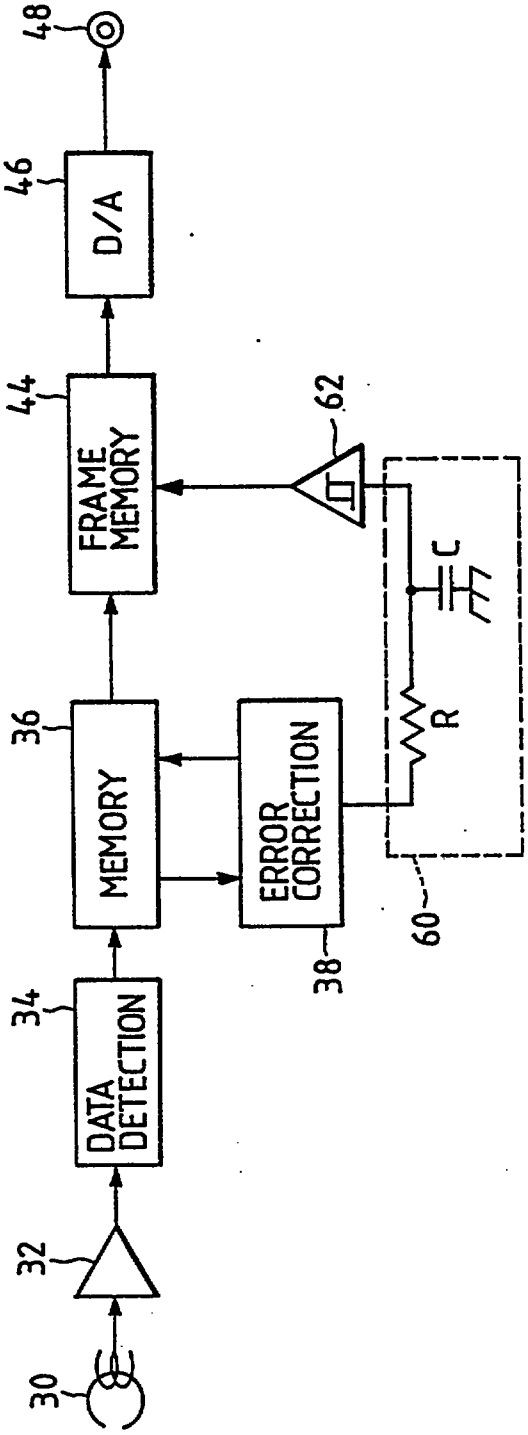
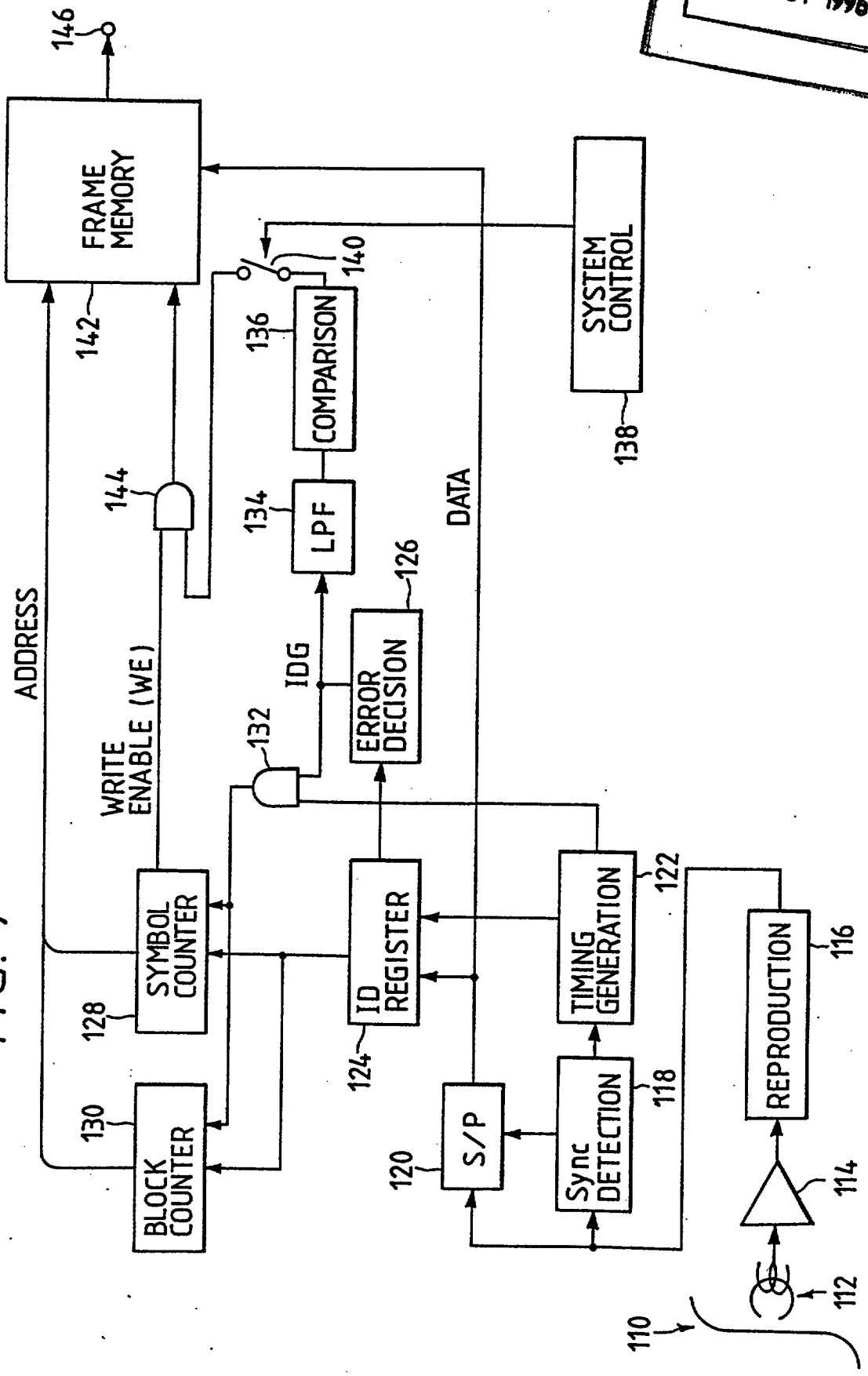


FIG. 6



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FIG. 7



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Claims

1. A device for receiving a digital data train including a video signal and generating therefrom an output video signal, the device comprising:

error detection means (38,126) for detecting errors in the received data train;
a memory (44,142) for storing video data defining an output video image frame; and
writing means (128,130) for writing video data extracted from the received data train into said memory so as to compose said output video image frame;

characterised by:

control means (40,42,60,62,122,128,132, 134,136,144) arranged to control the writing means with respect to each video image frame so as to write the video image frame into said memory (44, 142) if the error detection means indicates a predetermined low error rate; and not to write the video image frame into said memory (44, 142) if the error detection means indicates an error rate higher than the predetermined low error rate.

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2. A device according to claim 1, wherein said data train comprises a number of data blocks each having a video signal and an error detection or correction code, and wherein said error detection means is operable to detect the presence of a code error in each data block by using the associated error detection or correction code, and to output a flag in accordance with the detection result.

3. A device according to claim 2, wherein each data block includes an error correction parity word, and wherein said error detection means is operable to correct a code error within a data block using the associated parity word, and to output said flag in response to an occurrence of a data block having an uncorrectable error.

4. A device according to claim 2 or claim 3, wherein said control means includes a flag processing circuit (40,60,134,136) for detecting the occurrence frequency of said flag, and wherein the writing of each video image frame into said memory is controlled in accordance with the output from said flag processing circuit.

5. A device according to claim 4, wherein said flag processing circuit detects the occurrence frequency of said flag within a predetermined period.

6. A device according to claim 5, wherein said predetermined period corresponds to the frame period of said video signal.

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7. A device according to claim 5, wherein said flag processing circuit comprises a counter (40) for counting the number of occurrences of said flag generated during said predetermined period, and a comparator (42) for comparing the count value with a predetermined value.

8. A device according to claim 4, wherein said flag is a binary signal, and said flag processing circuit includes a circuit (60,134,136) for eliminating the high frequency components of said binary signal.

9. A device according to claim 8, wherein said eliminating circuit comprises a low-pass filter (60,134) to which said binary signal is inputted, and a comparator (62,135) for comparing the output from said low-pass filter with a predetermined value.

10. A device according to claim 9, wherein the output from said comparator changes from a first value to a second value when the output from said low-pass filter exceeds a first predetermined level, and from said second value to said first value when the output from said low-pass filter becomes smaller than a second predetermined level, said first predetermined level being higher than said second predetermined level.

11. A device according to any of preceding claims 2 to 10, wherein each data block includes allocation data representative of the position of said video signal

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12. A device according to claim 11, wherein said error detection or correction code is used for detecting an error in only said allocation data.

13. A device according to claim 1,2,4,6 or 8 further comprising:

mode changing means (138,140) for changing the operating mode of said device between first and second modes, the first mode being such that the control means controls writing of video image frames into said memory in accordance with the error rate indicated by the error detection means, and the second mode being such that video image frames are written irrespective of the error rate.

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Claims REPLACEMENT SHEET

1. A device for receiving a digital data train including a video signal and generating therefrom an output video signal, the device comprising:

error detection means (38,126) for detecting errors in the received data train;
a memory (44,142) for storing video data defining an output video image frame; and
writing means (128,130) for writing video data extracted from the received data train into said memory so as to compose said output video image frame;

characterised by:

control means (40,42,60,62,122,128,132, 134,136,144) arranged to control the writing means with respect to each video image frame so as to write the video image frame into said memory (44, 142) if the error detection means indicates a predetermined low error rate; and not to write the video image frame into said memory (44, 142) if the error detection means indicates an error rate higher than the predetermined low error rate.

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2. A device according to claim 1, wherein said data train comprises a number of data blocks each having a video signal and an error detection or correction code, and wherein said error detection means is operable to detect the presence of a code error in each data block by using the associated error detection or correction code, and to output a flag in accordance with the detection result.

3. A device according to claim 2, wherein each data block includes an error correction parity word, and wherein said error detection means is operable to correct a code error within a data block using the associated parity word, and to output said flag in response to an occurrence of a data block having an uncorrectable error.

4. A device according to claim 2 or claim 3, wherein said control means includes a flag processing circuit (40,60,134,136) for detecting the occurrence frequency of said flag, and wherein the writing of each video image frame into said memory is controlled in accordance with the output from said flag processing circuit.

5. A device according to claim 4, wherein said flag processing circuit detects the occurrence frequency of said flag within a predetermined period.

6. A device according to claim 5, wherein said predetermined period corresponds to the frame period of said video signal.

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7. A device according to claim 5, wherein said flag processing circuit comprises a counter (40) for counting the number of occurrences of said flag generated during said predetermined period, and a comparator (42) for comparing the count value with a predetermined value.

8. A device according to claim 4, wherein said flag is a binary signal, and said flag processing circuit includes a circuit (60,134,136) for eliminating the high frequency components of said binary signal.

9. A device according to claim 8, wherein said eliminating circuit comprises a low-pass filter (60,134) to which said binary signal is inputted, and a comparator (62,135) for comparing the output from said low-pass filter with a predetermined value.

10. A device according to claim 9, wherein the output from said comparator changes from a first value to a second value when the output from said low-pass filter exceeds a first predetermined level, and from said second value to said first value when the output from said low-pass filter becomes smaller than a second predetermined level, said first predetermined level being higher than said second predetermined level.

11. A device according to any of preceding claims 2 to 10, wherein each data block includes allocation data representative of the position of said video signal

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12. A device according to claim 11, wherein said error detection or correction code is used for detecting an error in only said allocation data.

13. A device according to claim 1,2,4,6 or 8 further comprising:

mode changing means (138,140) for changing the operating mode of said device between first and second modes, the first mode being such that the control means controls writing of video image frames into said memory in accordance with the error rate indicated by the error detection means, and the second mode being such that video image frames are written irrespective of the error rate.

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ABSTRACT:

DEVICE FOR PROCESSING TRANSMITTED DIGITAL VIDEO SIGNAL

A device for processing a digital code train including a video signal on a transmission line, wherein the write operation of the digital code train into a memory is controlled in accordance with an output from an error detection circuit for detecting a code error of the digital code train, thereby obtaining a good image even if some code of the digital code train is destroyed.

FIGURE 5

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