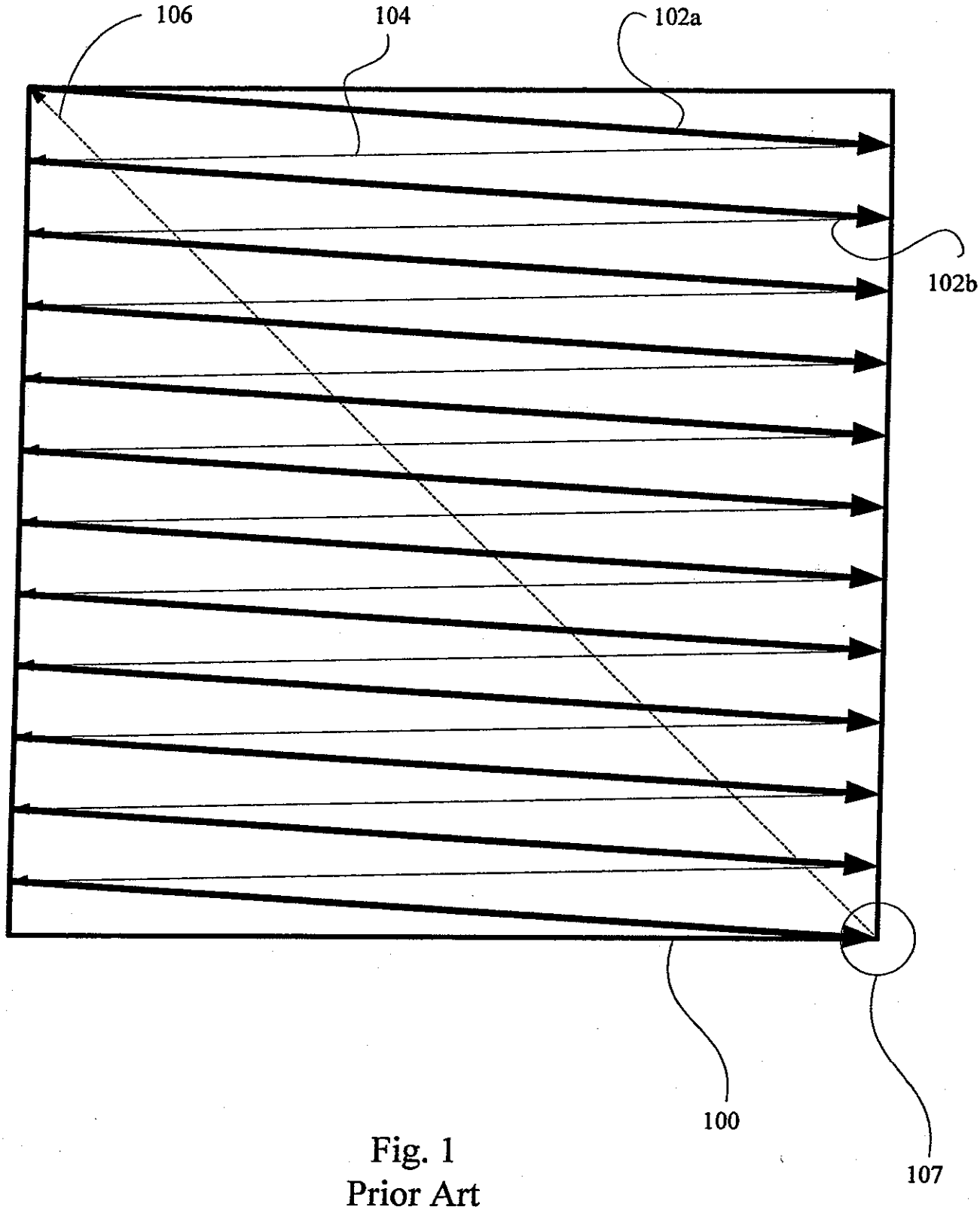


Fig. 1
Prior Art

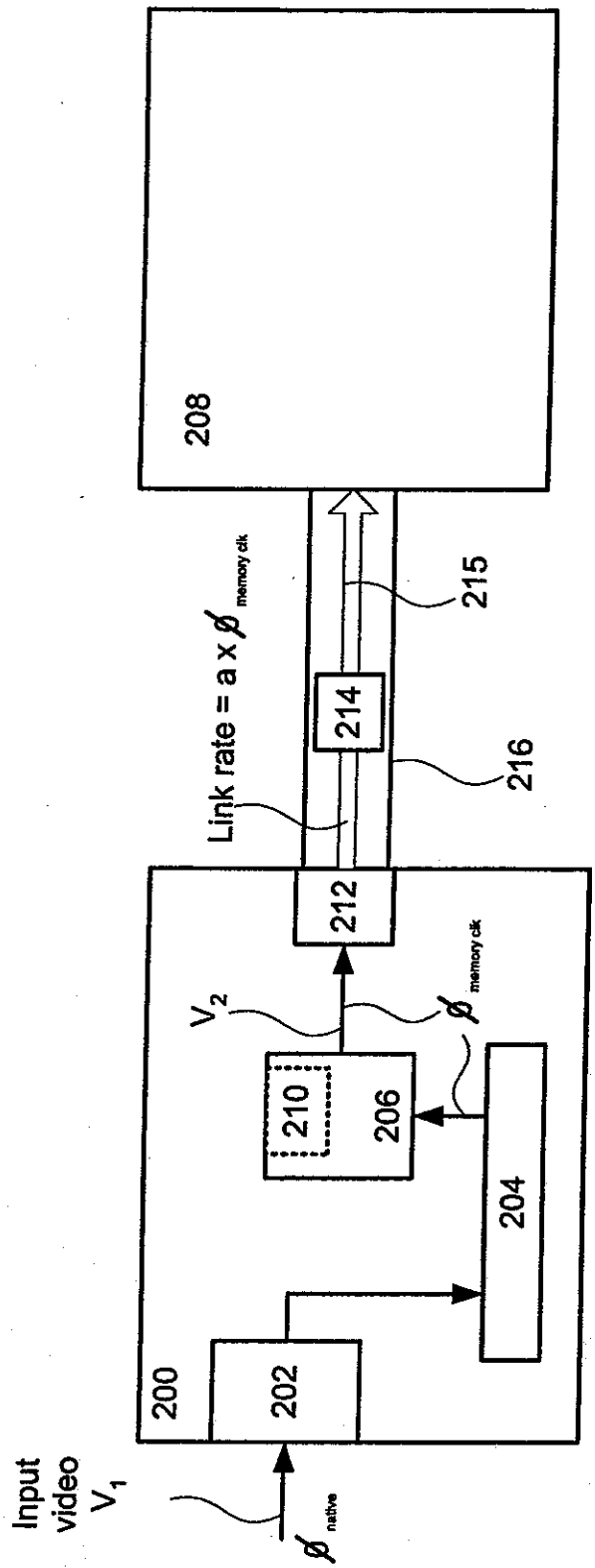

Input video V_1
ϕ_{native}
200
202
204
206
210
V_2
$\phi_{memory\ clk}$
212
Link rate = a x $\phi_{memory\ clk}$
214
215
216
208

Fig. 2

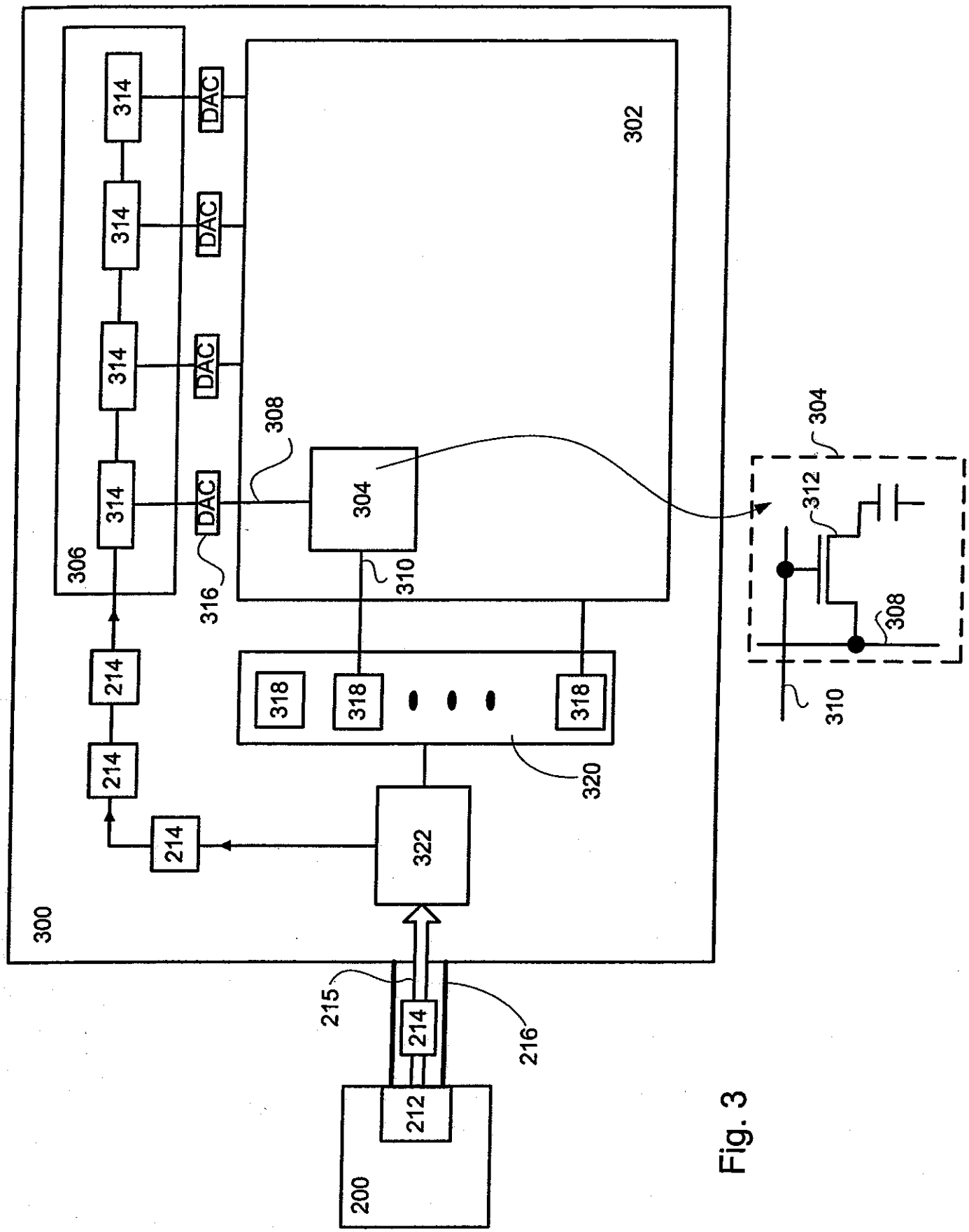

300
302
304
306
308
310
312
314
316
318
320
322
200
212
214
215
216
DAC

Fig. 3

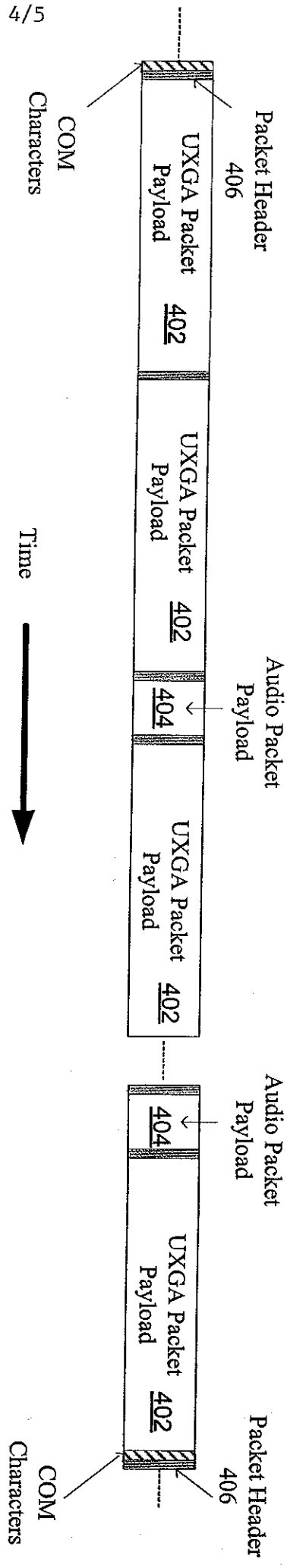

400
Packet Header
406
COM
Characters
UXGA Packet
Payload
402
UXGA Packet
Payload
402
404
Audio Packet
Payload
UXGA Packet
Payload
402
Time
404
Audio Packet
Payload
UXGA Packet
Payload
402
Packet Header
406
COM
Characters

Fig. 4

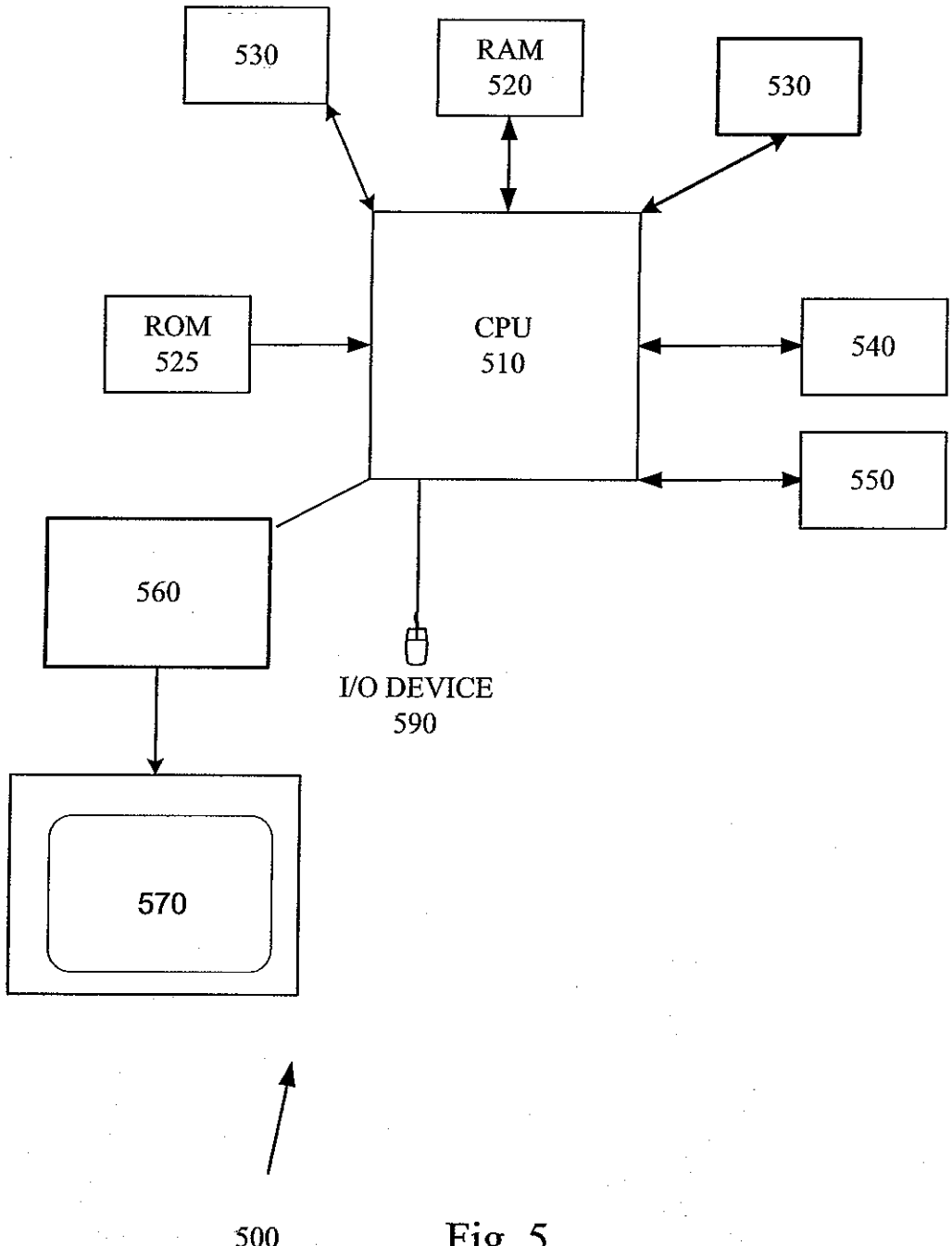

530
RAM
520
530
ROM
525
CPU
510
540
550
560
I/O DEVICE
590
570
500

Fig. 5