

CLAIMS

What is claimed is:

- 1 1. A method, comprising:
2 determining a desired logic state of a self-selecting memory cell, the desired
3 logic state representing more than one bit of data;
4 determining a polarity and an amplitude of a programming pulse based at least
5 in part on the desired logic state of the self-selecting memory cell; and
6 applying the programming pulse to the self-selecting memory cell based at
7 least in part on determining the polarity and the amplitude of the programming pulse.
- 1 2. The method of claim 1, wherein the self-selecting memory cell
2 comprises a chalcogenide alloy, a first side of the chalcogenide alloy interfacing with a first
3 electrode and a second side of the chalcogenide alloy interfacing with a second electrode, and
4 wherein the desired logic state of the self-selecting memory cell is associated with a threshold
5 voltage distribution and the threshold voltage distribution of the self-selecting memory cell is
6 set based at least in part on a local composition of the chalcogenide alloy.
- 1 3. The method of claim 2, wherein applying the programming pulse to the
2 self-selecting memory cell comprises:
3 modifying the local composition of the chalcogenide alloy by establishing an
4 electric field across the chalcogenide alloy and heating the chalcogenide alloy based at least
5 in part on the polarity and the amplitude of the programming pulse.
- 1 4. The method of claim 3, wherein at least one part of the chalcogenide
2 alloy includes silicon (Si), selenium (Se), arsenic (As), or germanium (Ge), the method
3 further comprising:
4 producing a net movement of the at least one part under the electric field to
5 alter the local composition of the chalcogenide alloy based at least in part on applying the
6 programming pulse to the self-selecting memory cell.
- 1 5. The method of claim 1, wherein the programming pulse comprises a
2 voltage difference applied to the self-selecting memory cell or a current flowing through the
3 self-selecting memory cell.

- 1 6. The method of claim 1, further comprising:
2 determining the polarity of the programming pulse based at least in part on a
3 present state of the self-selecting memory cell and the desired logic state of the self-selecting
4 memory cell.
- 1 7. The method of claim 1, further comprising:
2 setting a voltage amplitude of the programming pulse having the polarity to be
3 maintained during one or more durations; or
4 setting a current amplitude of the programming pulse associated with a first
5 electrode during one or more durations.
- 1 8. The method of claim 1, further comprising:
2 determining the polarity or the amplitude of the programming pulse based at
3 least in part on a current logic state of the self-selecting memory cell and the desired logic
4 state of the self-selecting memory cell, wherein the polarity and the amplitude define a shape
5 of the programming pulse.
- 1 9. The method of claim 1, wherein the programming pulse comprises:
2 a first voltage amplitude having a first polarity;
3 a second voltage amplitude having the first polarity;
4 the first voltage amplitude having a second polarity; or
5 the second voltage amplitude having the second polarity.
- 1 10. The method of claim 1, wherein the programming pulse comprises:
2 a first current amplitude of a current flowing from a first electrode;
3 a second current amplitude of the current flowing from the first electrode;
4 the first current amplitude of the current flowing to the first electrode; or
5 the second current amplitude of the current flowing to the first electrode.
- 1 11. A method, comprising:
2 identifying a read pulse having a plurality of voltages and a single polarity;
3 applying the read pulse to a self-selecting memory cell based at least in part on
4 identifying the read pulse;
5 detecting a threshold voltage of the self-selecting memory cell based at least in
6 part on applying the read pulse; and

7 determining a logic state of the self-selecting memory cell based at least in
8 part on detecting the threshold voltage of the self-selecting memory cell, the logic state
9 representing more than one bit of data.

1 12. The method of claim 11, further comprising:
2 programming the self-selecting memory cell using a programming pulse
3 having a same polarity as the read pulse.

1 13. The method of claim 11, further comprising:
2 programming the self-selecting memory cell using a programming pulse
3 having a different polarity than the read pulse.

1 14. The method of claim 11, wherein the read pulse has a constant rate of
2 increase in voltage with respect to time within a predetermined voltage range.

1 15. The method of claim 14, wherein the predetermined voltage range is
2 associated with a range of the threshold voltage of the self-selecting memory cell storing
3 more than one bit of data.

1 16. The method of claim 11, wherein the read pulse comprises a plurality
2 of durations, each duration of the plurality of durations associated with a voltage of the
3 plurality of voltages.

1 17. A method, comprising:
2 determining a desired threshold voltage of a self-selecting memory cell that
3 comprises a chalcogenide alloy, a first side of the chalcogenide alloy interfacing with a first
4 electrode and a second side of the chalcogenide alloy interfacing with a second electrode, and
5 the desired threshold voltage corresponding to a desired logic state of the self-selecting
6 memory cell representing more than one bit of data;
7 determining a polarity and an amplitude of a programming pulse based at least
8 in part on the desired threshold voltage of the self-selecting memory cell; and
9 altering a spatial distribution of at least one part of the chalcogenide alloy by
10 applying the programming pulse to the self-selecting memory cell based at least in part on
11 determining the polarity and the amplitude of the programming pulse, wherein the desired
12 threshold voltage of the self-selecting memory cell is based at least in part on the spatial
13 distribution of at least one part of the chalcogenide alloy.

1 18. The method of claim 17, wherein determining the polarity and the
2 amplitude of the programming pulse comprises:
3 setting the polarity of the programming pulse based at least in part on a present
4 state of the self-selecting memory cell and the desired logic state of the self-selecting memory
5 cell; and
6 setting a current amplitude of the programming pulse having a first polarity to
7 be maintained during one or more durations.

1 19. The method of claim 17, wherein applying the programming pulse to
2 the self-selecting memory cell comprises:
3 initiating net movements of the at least one part of the chalcogenide alloy
4 using an electric field across the chalcogenide alloy based at least in part on the polarity and
5 the amplitude of the programming pulse; and
6 initiating a temperature change of the chalcogenide alloy based at least in part
7 on a current flowing through the self-selecting memory cell.

1 20. The method of claim 17, further comprising:
2 setting the desired threshold voltage of the self-selecting memory cell based at
3 least in part on a concentration of the at least one part of the chalcogenide alloy at a first
4 interface of the self-selecting memory cell.

1 21. A method, comprising:
2 determining a desired logic state of a self-selecting memory cell comprising a
3 chalcogenide alloy, the desired logic state representing more than one bit of data;
4 determining a shape of a programming pulse based at least in part on the
5 desired logic state of the self-selecting memory cell; and
6 applying the programming pulse to the self-selecting memory cell based at
7 least in part on determining the shape of the programming pulse.

1 22. The method of claim 21, wherein determining the shape of the
2 programming pulse comprises:
3 determining one or more durations during which a fixed voltage amplitude
4 having a first polarity is maintained.

1 23. The method of claim 22, further comprising:
2 varying the shape of the programming pulse to change a strength, or a
3 direction, or both of an electric field across the chalcogenide alloy during each duration when
4 the programming pulse is applied to the self-selecting memory cell; and
5 heating the chalcogenide alloy using a current flowing through the self-
6 selecting memory cell under the electric field during at least one duration when the
7 programming pulse is applied.

1 24. The method of claim 21, wherein the self-selecting memory cell
2 comprises a first interface between a first electrode in contact with a first side of the
3 chalcogenide alloy and a second interface between a second electrode in contact with a
4 second side of the chalcogenide alloy, and wherein applying the programming pulse to the
5 self-selecting memory cell further comprises:
6 producing a current flowing through the chalcogenide alloy;
7 heating the chalcogenide alloy based at least in part on producing the current;
8 and
9 initiating a net movement of at least one part of the chalcogenide alloy
10 between the first side of the chalcogenide alloy and the second side of the chalcogenide alloy
11 based at least in part on heating the chalcogenide alloy.

1 25. A memory device, comprising:
2 a cross-point memory array comprising self-selecting memory cells;
3 a controller coupled with the cross-point memory array, the controller being
4 operable to:
5 determine a desired logic state of a self-selecting memory cell, the
6 desired logic state representing more than one bit of data;
7 determine a polarity and an amplitude of a programming pulse based at
8 least in part on the desired logic state of the self-selecting memory cell; and
9 apply the programming pulse to the self-selecting memory cell based at
10 least in part on determining the polarity and the amplitude of the programming pulse.

1 26. The memory device of claim 25, wherein the self-selecting memory
2 cell comprises a chalcogenide alloy, a first side of the chalcogenide alloy interfacing with a
3 first electrode and a second side of the chalcogenide alloy interfacing with a second

4 electrode, and wherein the desired logic state of the self-selecting memory cell is associated
5 with a threshold voltage distribution and the threshold voltage distribution of the self-
6 selecting memory cell is set based at least in part on a local composition of the chalcogenide
7 alloy.

1 27. The memory device of claim 26, wherein the controller is further
2 operable to:

3 modify the local composition of the chalcogenide alloy by establishing an
4 electric field across the chalcogenide alloy and heating the chalcogenide alloy based at least
5 in part on the polarity and the amplitude of the programming pulse.

1 28. The memory device of claim 25, wherein the controller is further
2 operable to:

3 determine the polarity of the programming pulse based at least in part on a
4 present state of the self-selecting memory cell and the desired logic state of the self-selecting
5 memory cell.

1 29. The memory device of claim 25, wherein the controller is further
2 operable to:

3 set a voltage amplitude of the programming pulse having the polarity to be
4 maintained during one or more durations; or

5 set a current amplitude of the programming pulse associated with an electrode
6 during one or more durations.

1 30. The memory device of claim 29, further comprising:

2 a periphery circuit that produces the polarity of the programming pulse.