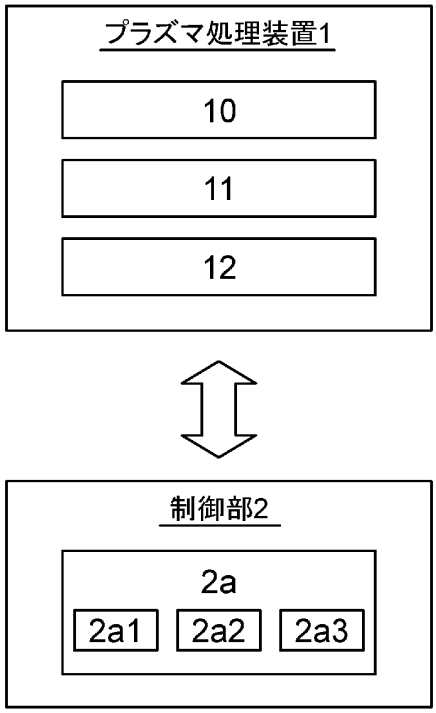
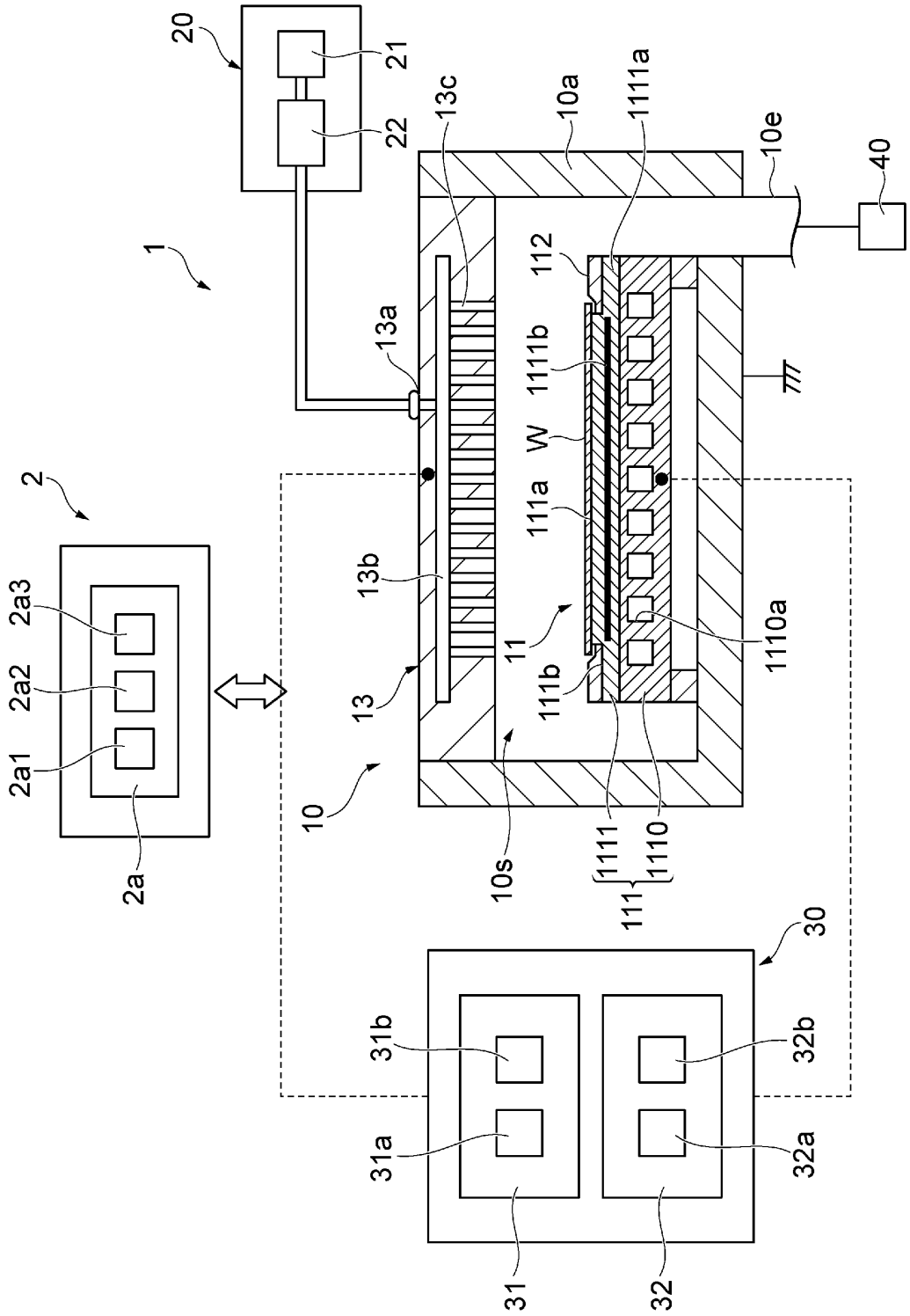
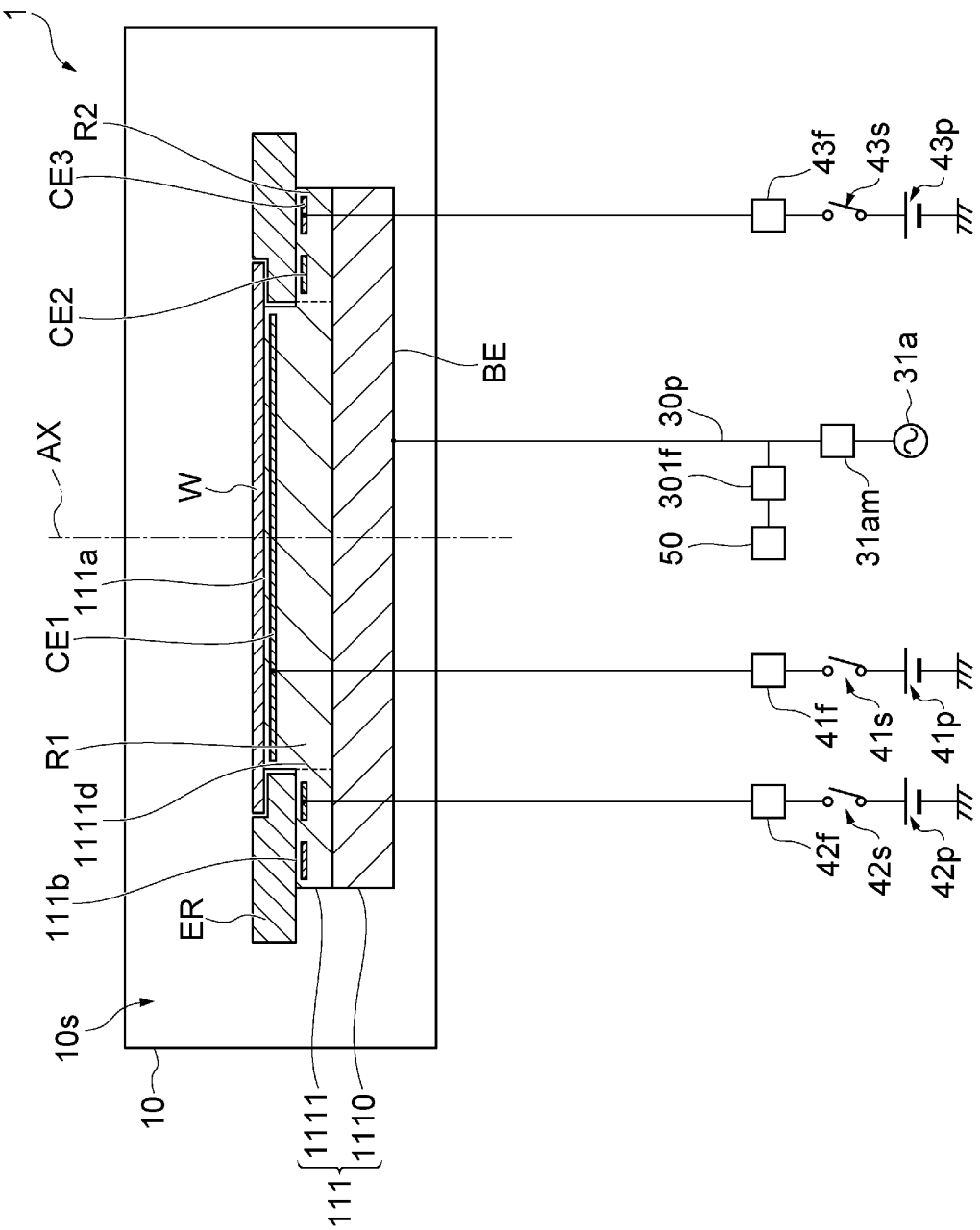
[図1]



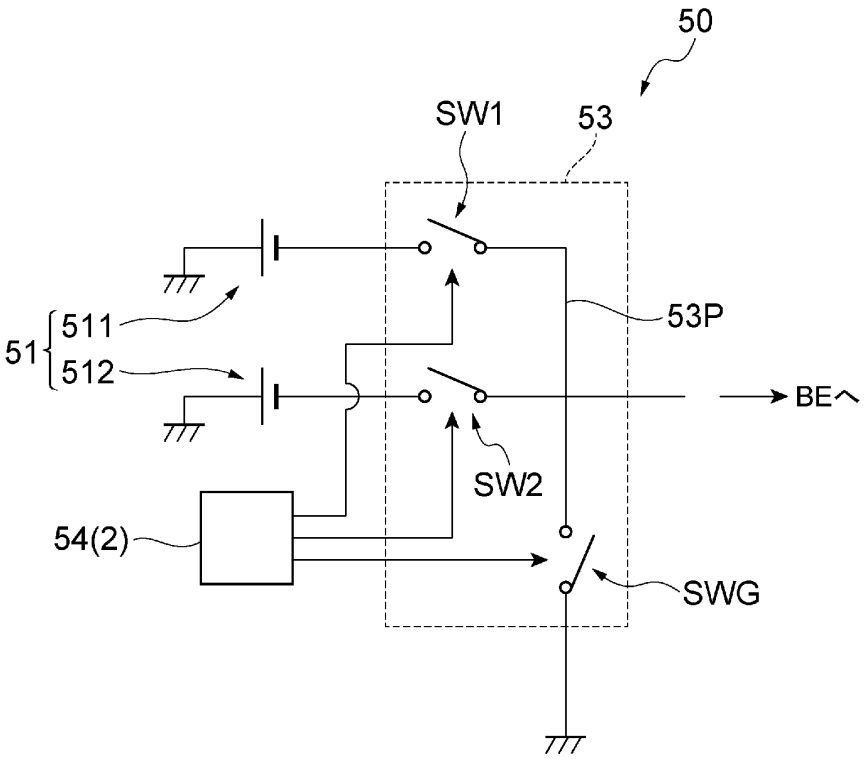
[図2]


20
21
22
13c
10a
1111a
10e
40
1
112
13a
1111b
W
111a
13b
11
1110a
111b
13
10
10s
1111
1110
111
30
31b
32b
31a
32a
31
32
2
2a3
2a2
2a1
2a

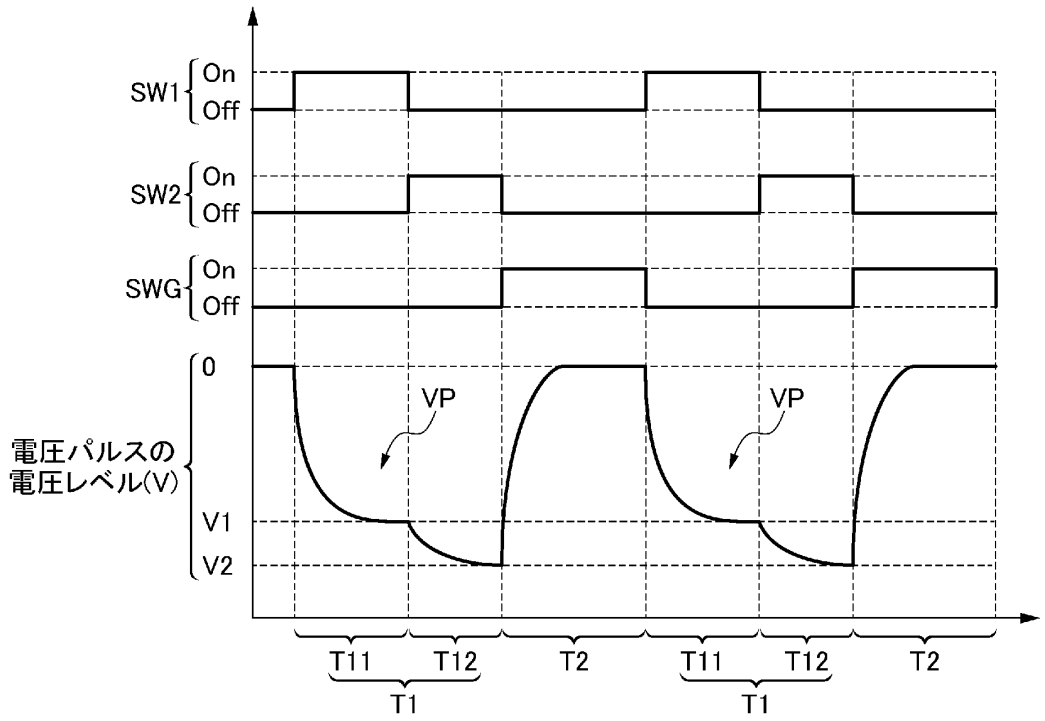
[図3]


1
R2
CE3
CE2
AX
W
CE1
111a
R1
1111d
111b
ER
10s
10
1111
1110
111
BE
43f
43s
43p
30p
31a
301f
50
31am
41f
41s
41p
42f
42s
42p

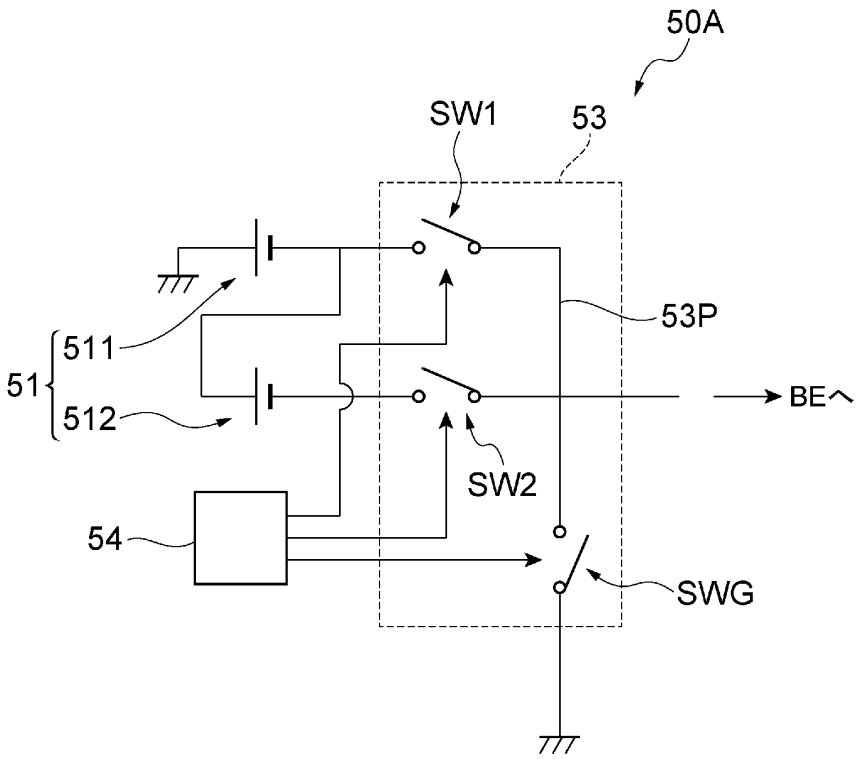
[図4]



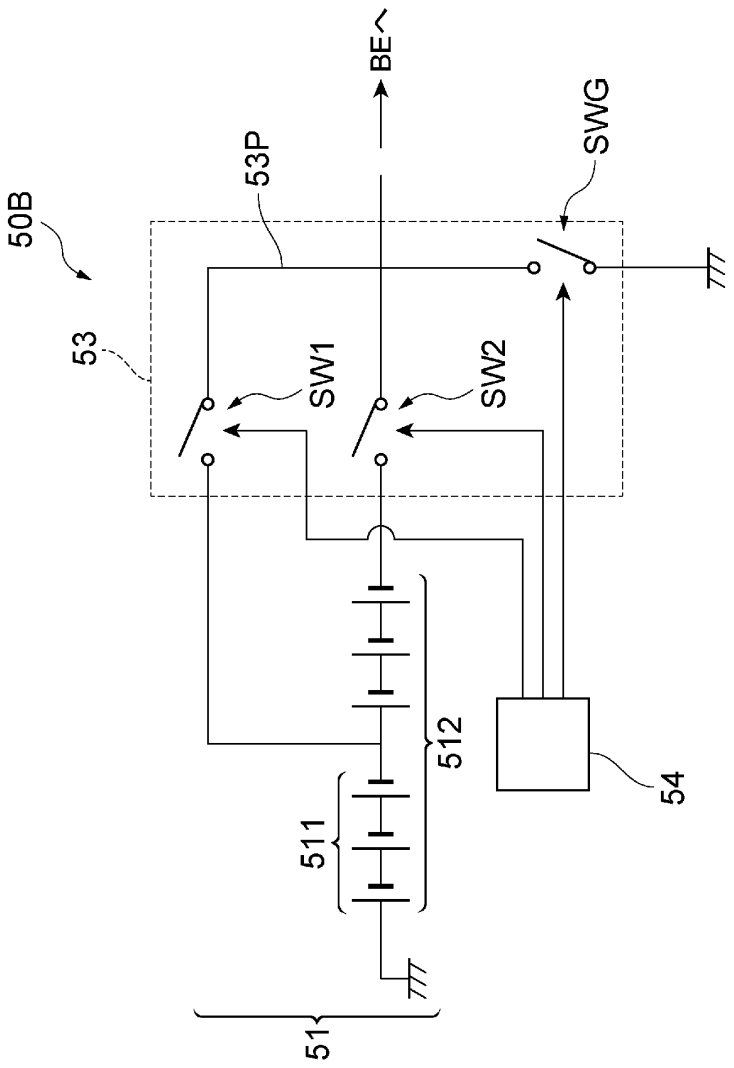
[図5]


SW1
On
Off
SW2
On
Off
SWG
On
Off
電圧パルスの
電圧レベル(V)
0
V1
V2
VP
VP
T11
T12
T2
T11
T12
T2
T1
T1

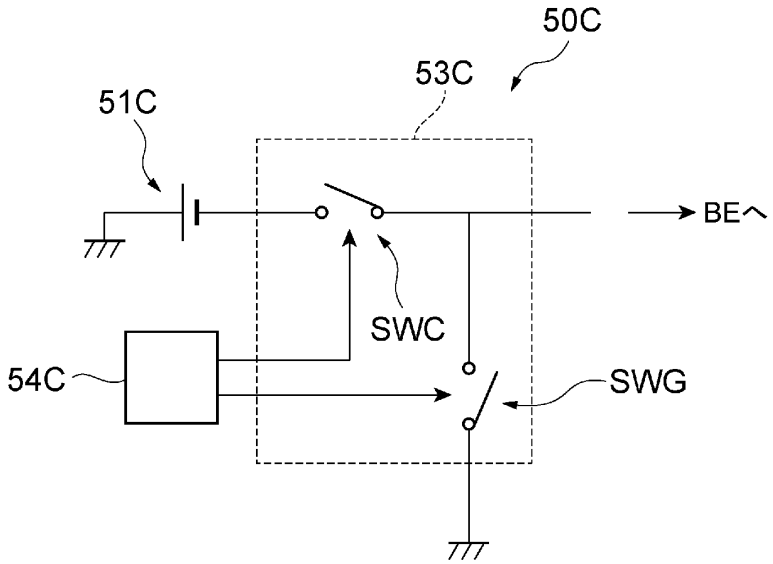
[図6]



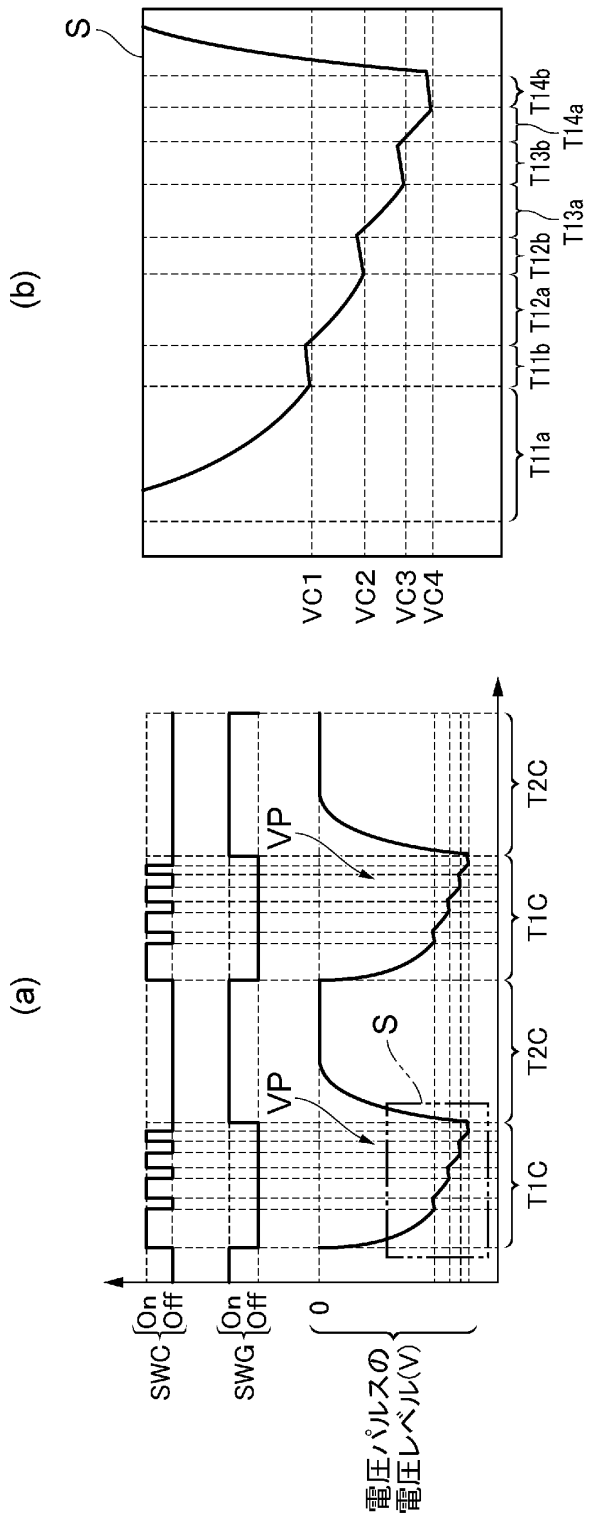
[図7]



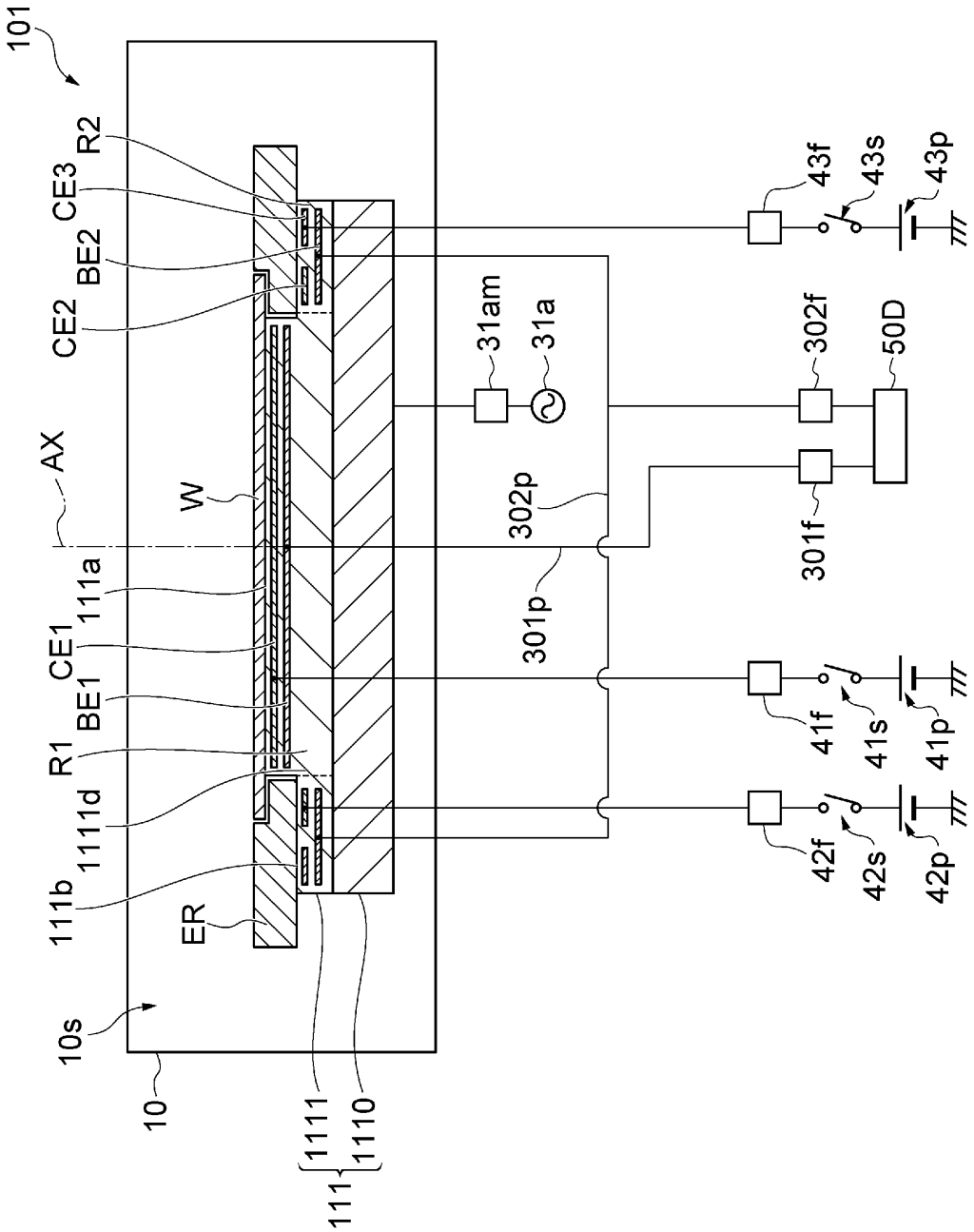
[図8]



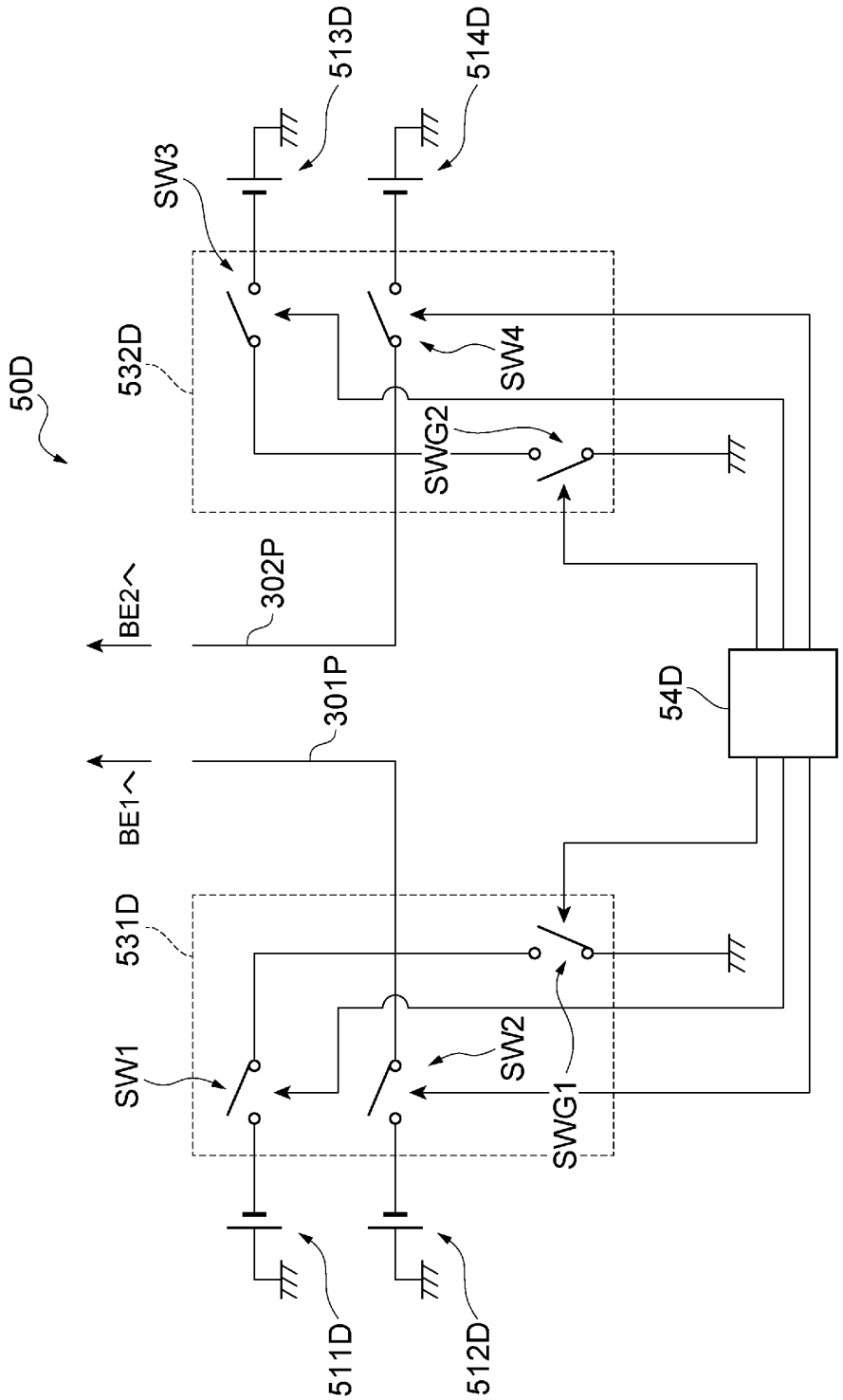
[図9]


(a)
SWC
On
Off
SWG
On
Off
0
電圧パルスの
電圧レベル(V)
VP
VP
S
T1C
T2C
T1C
T2C
(b)
S
VC1
VC2
VC3
VC4
T11a
T11b
T12a
T12b
T13a
T13b
T14a
T14b

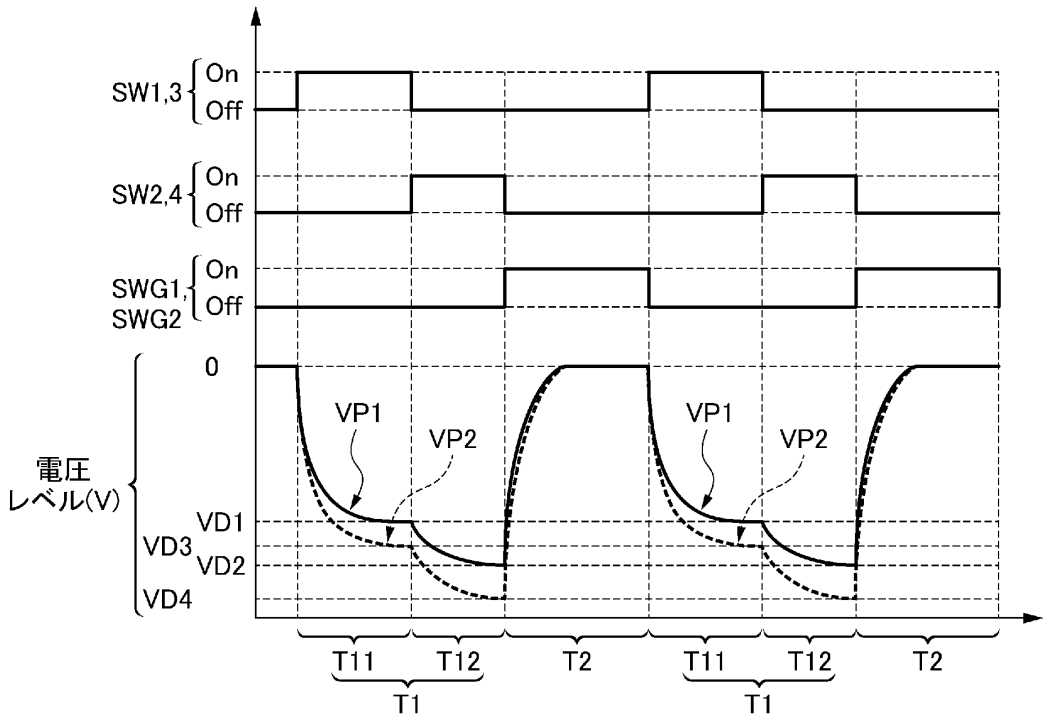
[図10]


101
R2
CE3
BE2
CE2
AX
W
111a
CE1
BE1
R1
1111d
111b
ER
10s
10
1111
1110
111
31am
31a
302p
301p
43f
43s
43p
302f
50D
301f
41f
41s
41p
42f
42s
42p

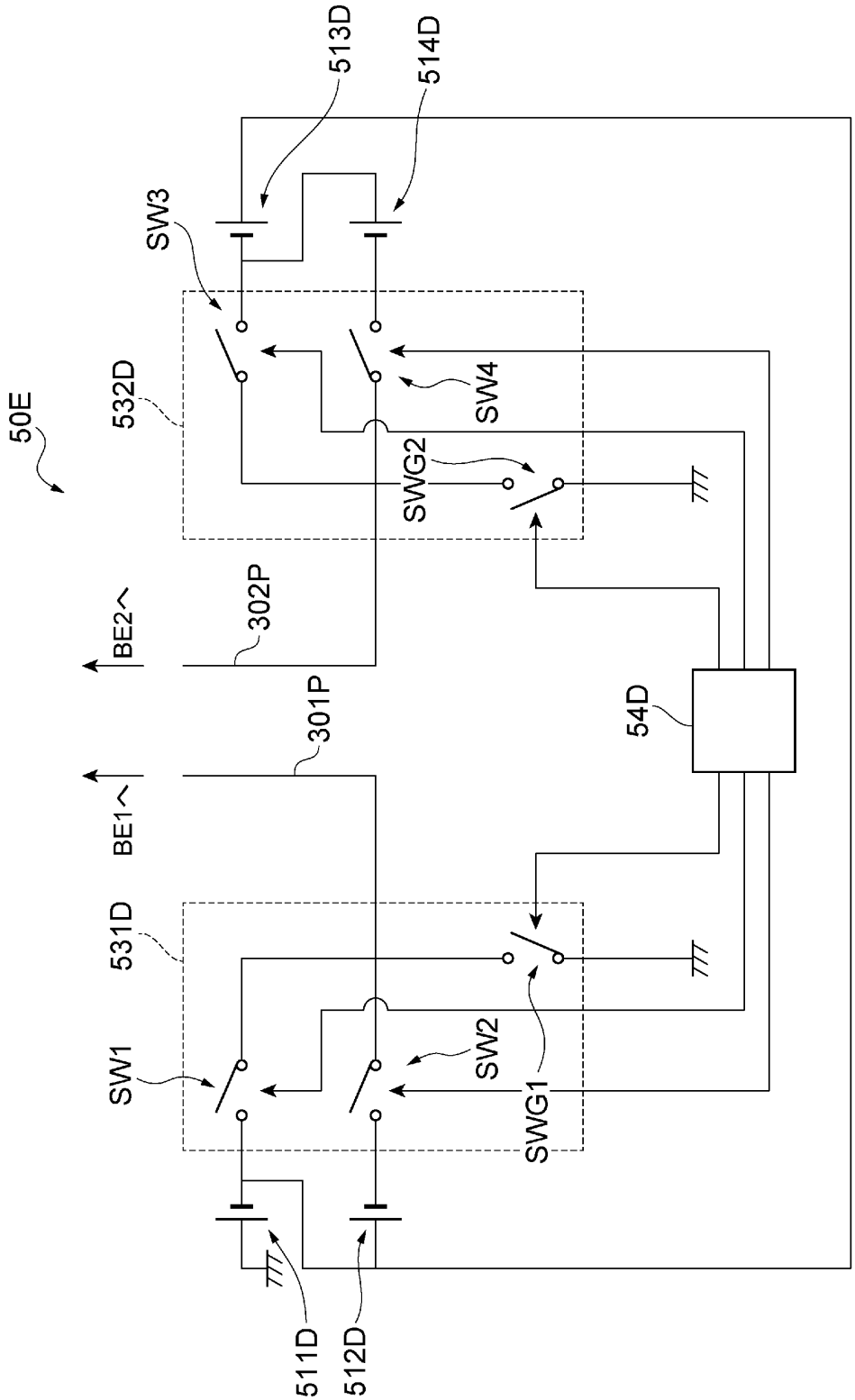
[図11]


50D
532D
513D
514D
SW3
SW4
SWG2
302P
BE2へ
301P
BE1へ
54D
531D
SW1
SW2
SWG1
511D
512D

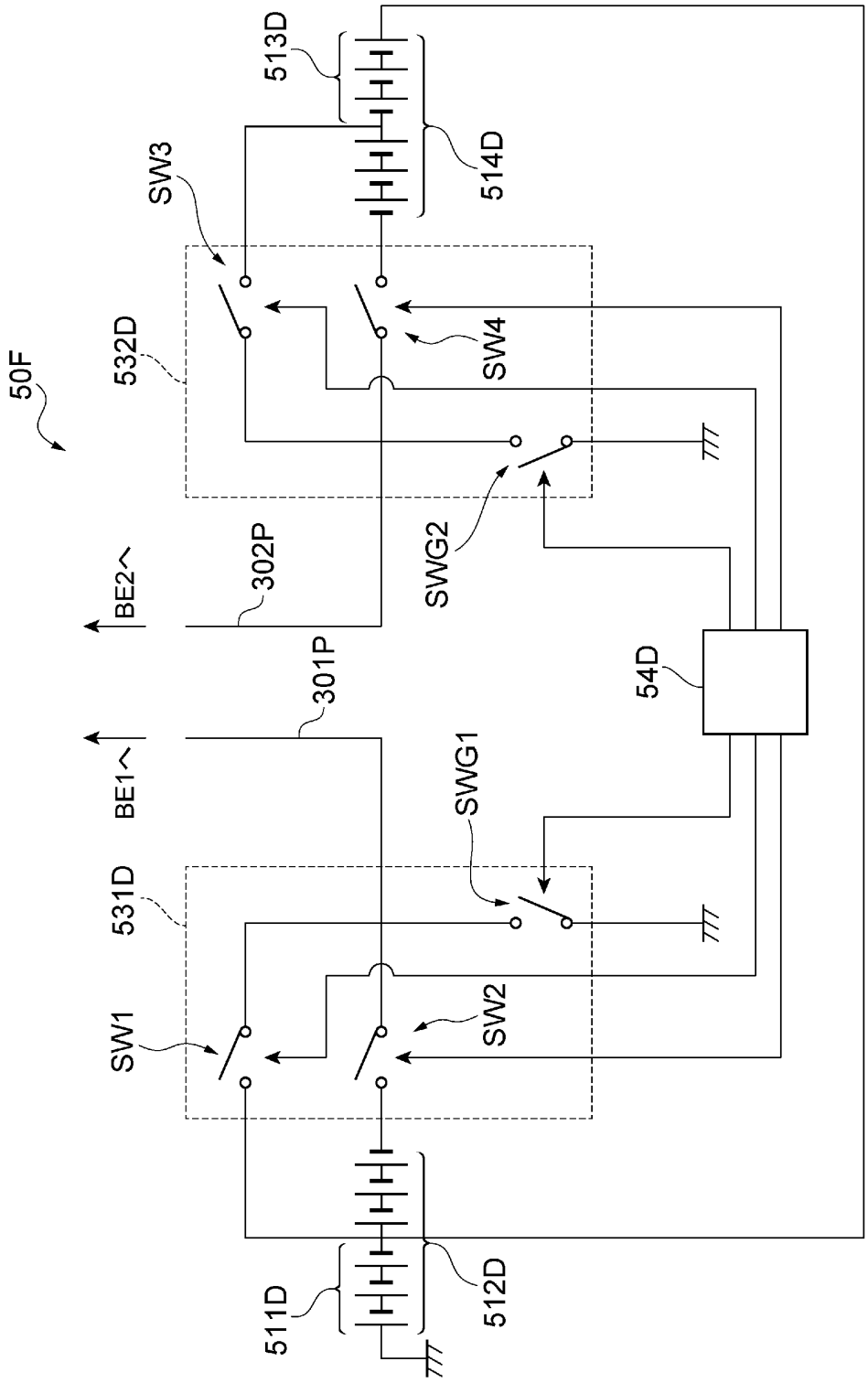
[図12]


SW1,3
On
Off
SW2,4
On
Off
SWG1,
SWG2
On
Off
電圧
レベル(V)
0
VP1
VP2
VP1
VP2
VD1
VD3
VD2
VD4
T11
T12
T2
T11
T12
T2
T1
T1

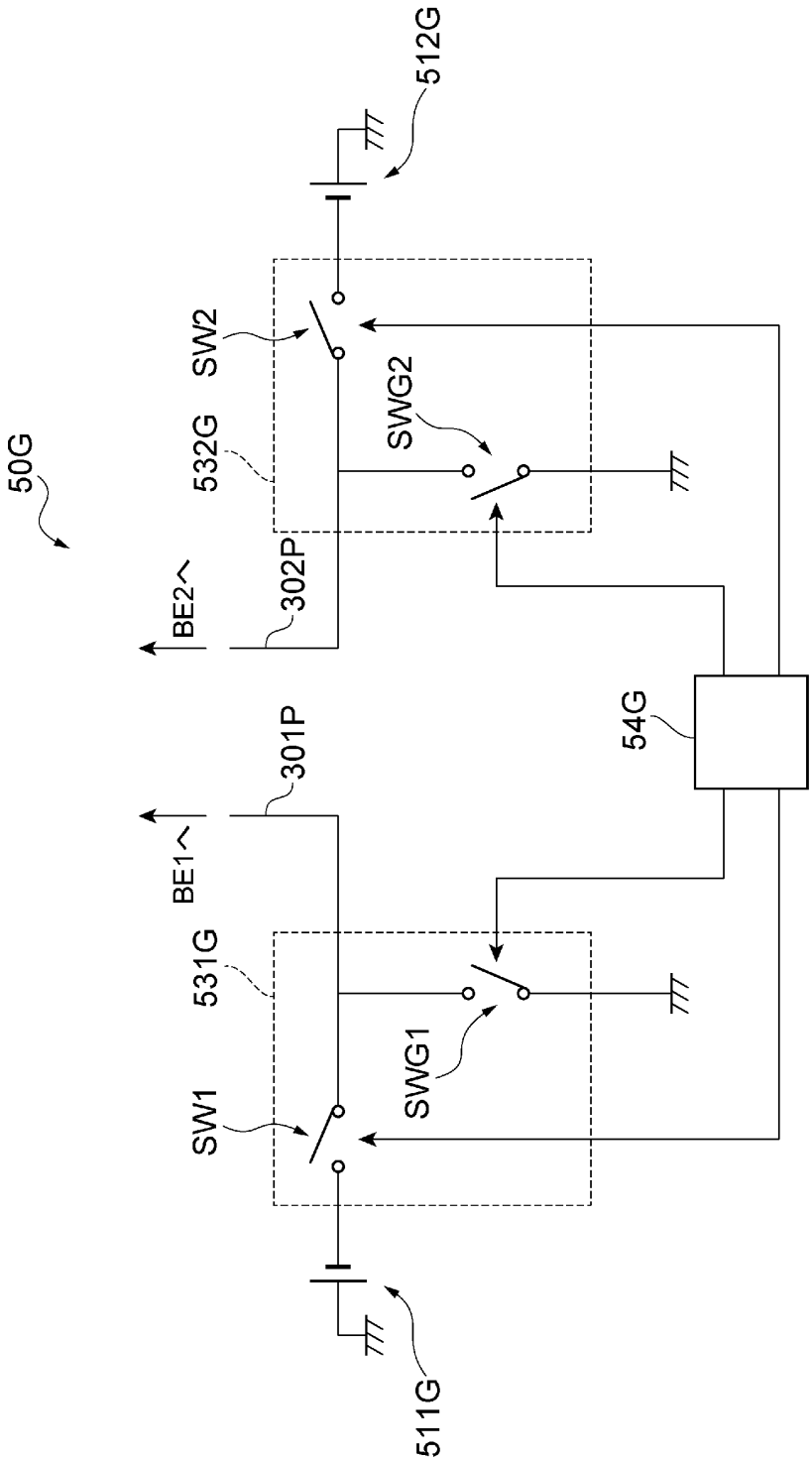
[図13]


513D
514D
SW3
SW4
532D
50E
SWG2
302P
BE2へ
301P
54D
BE1へ
531D
SW1
SW2
SWG1
511D
512D

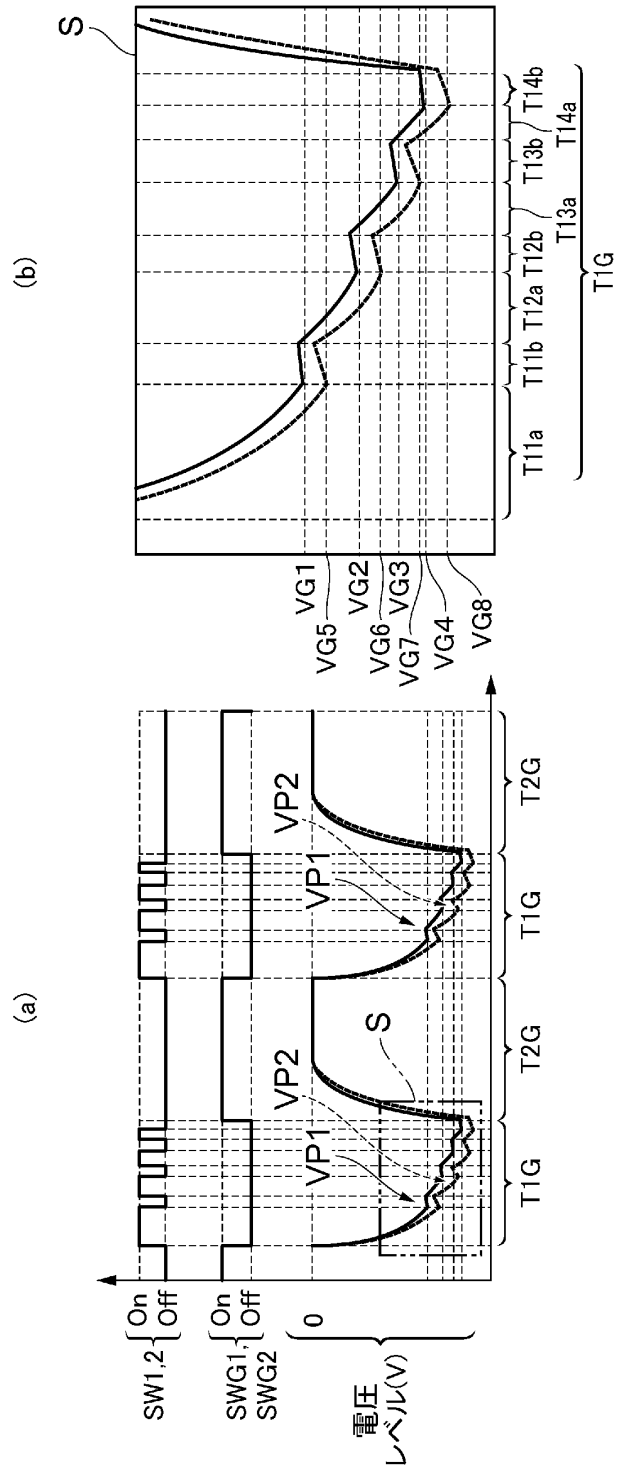
[図14]


50F
513D
514D
SW3
SW4
532D
SWG2
302P
BE2へ
301P
54D
BE1へ
SWG1
531D
SW1
SW2
511D
512D

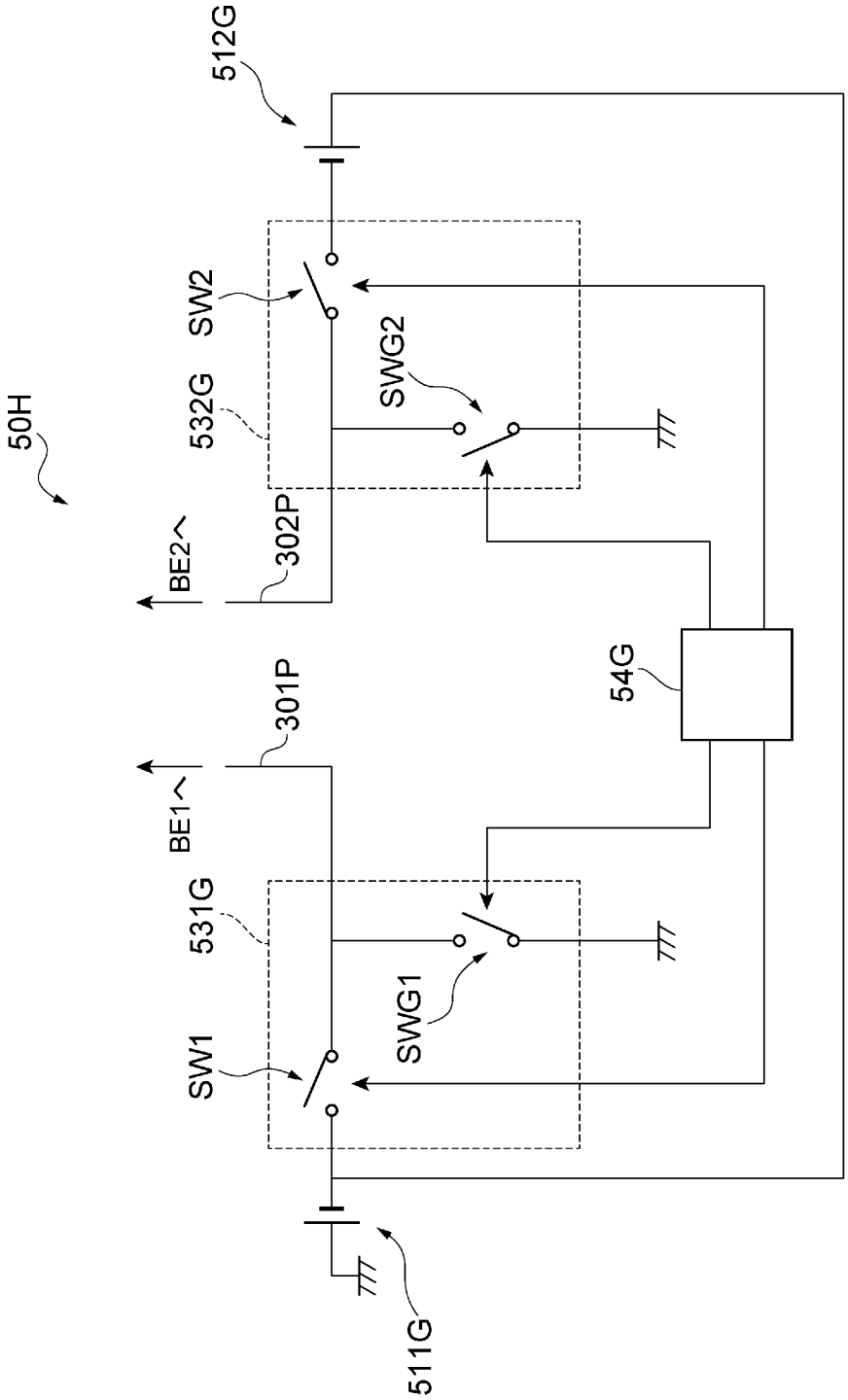
[図15]


512G
SW2
SWG2
532G
50G
BE2^
302P
54G
301P
BE1^
531G
SWG1
SW1
511G

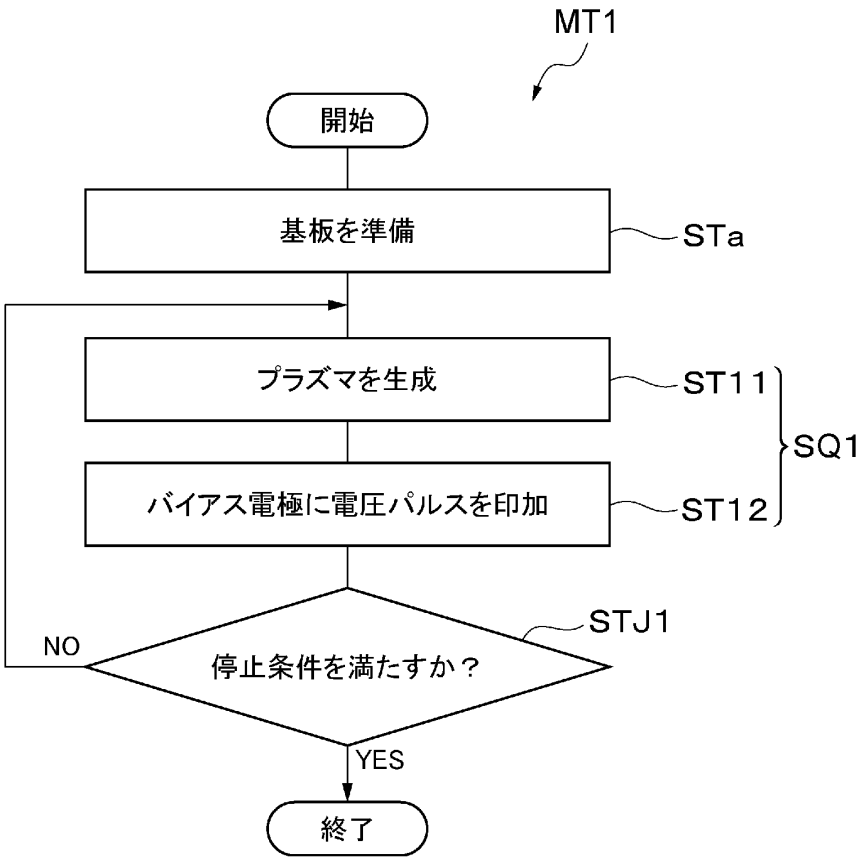
[図16]


(a)
(b)
SW1,2
On
Off
SWG1,
SWG2
On
Off
0
電圧
レベル(V)
VP1
VP2
VP1
VP2
S
S
T1G
T2G
T1G
T2G
T1G
T11a
T11b
T12a
T12b
T13a
T13b
T14a
T14b
VG1
VG2
VG3
VG4
VG5
VG6
VG7
VG8

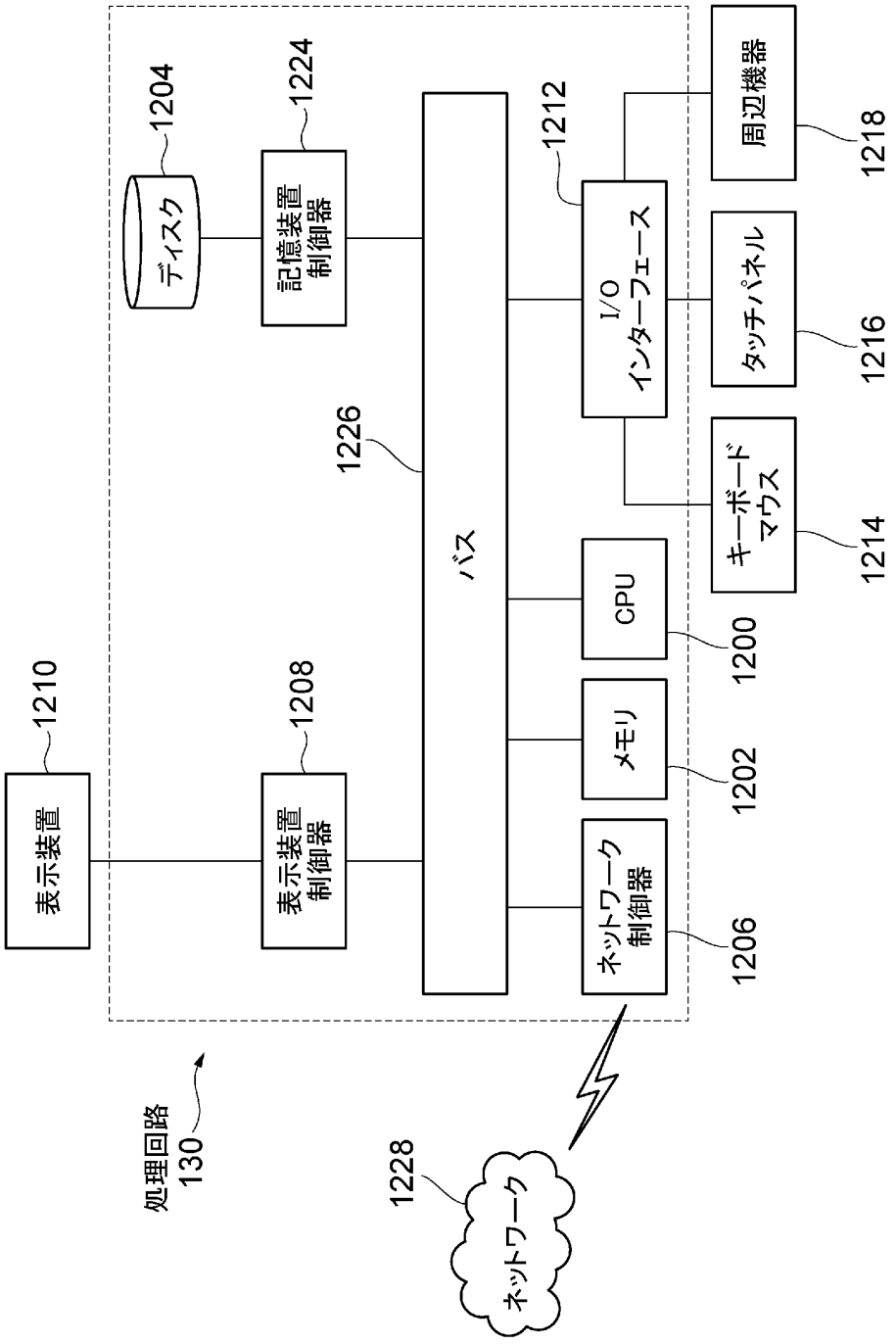
[図17]


512G
SW2
SWG2
532G
50H
BE2^
302P
54G
301P
BE1^
531G
SWG1
SW1
511G

[図18]


MT1
開始
基板を準備
STa
プラズマを生成
ST11
バイアス電極に電圧パルスを印加
ST12
SQ1
停止条件を満たすか？
STJ1
NO
YES
終了

[図19]


処理回路
130
1228
ネットワーク
1206
ネットワーク
制御器
1202
メモリ
1200
CPU
1214
キーボード
マウス
1216
タッチパネル
1218
周辺機器
1210
表示装置
1208
表示装置
制御器
1226
バス
1212
I/O
インターフェース
1224
記憶装置
制御器
1204
ディスク