

ABSTRACT



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Clock Recovery Apparatus



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An out of lock condition is sensed on a data transition basis in clock recovery apparatus. When an out of lock condition is sensed (by false lock detector 20), a range sweeping signal is generated (by one shot 21) and summed with the correction signal (across capacitor 16) to sweep the frequency of the block signal over the frequency range of the VCO. When an out of lock condition is absent, i.e., when the VCO is phase locked, simulated data transitions are generated in the frequency/phase detector (by an exclusive OR gate). An out of lock condition is sensed by a D flip-flop. Data is coupled to the clock input of the flip-flop, the clock signal is delayed by a fraction of its nominal period (by delaying amplifier 23) and coupled to the D input of the flip-flop. The state of the Q output of the flip-flop indicates an out of lock condition. The controlled oscillator may include a number of series connected delay stages and also be associated with a temperature compensating circuit.

(Figure 1)