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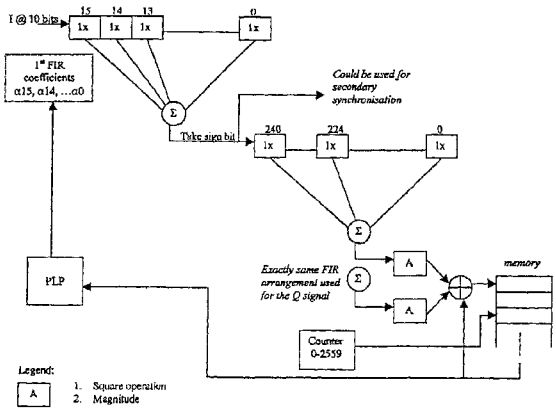
(54) Title: HIGH PERFORMANCE W-CDMA SLOT SYNCHRONISATION FOR INITIAL CELL SEARCH WITH REDUCED HARDWARE



(57) Abstract: The present invention outlines two preferred embodiements for slot synchronisation of an initial cell search for Third-Generation Partnership Project (3GPP) Wideband Code-Division Multiple Access (W-CDMA) Frequency Division Duplex (FDD) mode system. Two Finite Impulse Response (FIR) filters are used to correlate the synchronisation codes transmited in the downlink (forward link). Sign bit is taken after the first FIR to significantly reduced the hardware requirements for the second FIR, and thus the whole system. The same hardware is repeated for the real (I) and imaginary (Q) parts of the signal before the subsequent processes. The correlated results from the second FIR can be further processed using two different alogrithms. The first is to add a square operation to the correlated results whilst the second is to take the magnitude before passing to the next stage. Regardless of which algorithm is adopted, the results are accumulated (I and Q), instead of averaged, and stored in a memory location for each successive correlation over the same location in different slots. The physical-layer processor (PLP) then reads the accumulated results from the memory location and searches for the peak position. This peak position corresponds to the actual slot boundary.

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