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INSULATED GATE SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING SAME

The present invention relates to an insulated gate semiconductor device having an insulated gate field effect transistor and a protective element for protecting the transistor. It also relates to a method of fabricating such a device.

In the following description the insulated gate field effect transistor will be referred to as a 'MOSFET'.

It is usual to form the protective element as a diode in the semiconductor substrate also containing the MOSFET. However, in UK Patent Specification No. 1380466 there is disclosed a device in which a MOSFET is formed as part of a substrate with a gate electrode in the form of a semiconductor layer separated from the substrate by an insulating film. Another semiconductor layer forming the protective element is also separated from the substrate by the insulating film.

However, the parts of the insulating film separating the substrate from the gate electrode and the protective device are of the same thickness and this leads to problems which will be discussed later.

Therefore a first aspect of the present invention provides an insulated gate semiconductor device having an insulated gate field effect transistor forming part of a substrate and a protective element for protecting the gate electrode of the transistor, the protective element and the gate electrode being semiconductor layers integral with each other on an insulating film on the surface of the substrate, the part of the insulating film separating the semiconductor layer of the protective element from the substrate being thicker than the part of the insulating film separating the semiconductor layer of the gate electrode from the substrate.

Preferably, the transistor has a drain region of a

first conductivity type, a channel region of a second conductivity type in the drain region, and a source region of the first conductivity type in the channel region. The protective element prevents dielectric breakdown of the gate insulating film.

The semiconductor layer forming the protective element may have one or more P-N junctions formed therein, and preferably the P-N junction(s) are shaped in such a manner that their cross-sections are not exposed.

According to a second aspect of the present invention there is provided a method of fabricating an insulated gate semiconductor device including:

forming an insulated gate field effect transistor in a substrate,

forming an insulating film on a surface of the substrate, the insulating film having a first part and a second part thicker than the first part, and

forming integral semiconductor layers on the insulating film, the semiconductor layer on the thinner part of the insulating film being located relative to the transistor such that it forms a gate electrode, the semiconductor layer on the thicker part of the insulating film forming a protective device for protecting the gate electrode of the transistor.

Preferably, the formation of the transistor includes:

introducing an impurity of a second conductivity type into the substrate using a part of the semiconductor layer on the thinner part of the insulating film as a mask, the substrate being of a first conductivity type, to form a channel region in parts of the substrate forming a drain region; and

introducing an impurity of the first conductivity type into the channel region, using a part of the semiconductor layer on the thinner part of the insulating film as a mask, to form a source region in the channel region.

Embodiments of the invention will now be described in detail, by way of example, with reference to the accompanying

drawings, in which:

Fig. 1 is a sectional view of the principal portions of an N channel vertical MOSFET being a first embodiment of the present invention;

Fig. 2 is an equivalent circuit diagram of the N channel vertical MOSFET of Fig. 1;

Fig. 3 is a plan view of the semiconductor chip and shows the disposition of the protective element;

Fig. 4 is a plan view of the chip as a whole and shows the disposition of the electrodes when the semiconductor device is completed;

Fig. 5 is a sectional view of the polycrystalline Si layer which serves as the protective element;

Fig. 6 is the current vs. voltage characteristic curve of the protective element;

Fig. 7 is a schematic perspective view and shows the relation between the protective element and the gate electrode of the MOSFET;

Fig. 8a to 8h are sectional views and show a preferred fabrication process of the vertical MOSFET in accordance with the present invention;

Fig. 9 is a partial sectional view of a protective element fabricated by another fabrication method;

Fig. 10 is a partial sectional view and shows a protective element formed by still another fabrication method;

Fig. 11 is a schematic perspective view and shows an example of a modification of the protective element;

Fig. 12 is a partial sectional view and shows another example of a modification of the protective element;

Fig. 13 is a schematic perspective view and shows still another example of a modification of the protective element; and

Fig. 14 is an equivalent circuit diagram of the N-channel vertical MOSFET corresponding to Fig. 13.

Figure 1 is a sectional view of an N-channel vertical MOSFET being a first embodiment of the present invention.

In the drawing, the direction indicated by arrow A represents the central portion of a semiconductor pellet

where principal portions of a vertical MOSFET are formed by epitaxial growth. The direction indicated by arrow B represents the peripheral portion of the semiconductor pellet. In the vertical MOSFET shown in Figure 1, an N^- semiconductor (N^-silicon) layer 2 is formed on one main surface of an N^+ semiconductor (N^+ silicon) substrate 1. This N^+ semiconductor substrate 1 and N^- semiconductor layer 2 function as the drain region of the MOSFET. P well regions 3, 30, 31 are selectively formed inside this N^- semiconductor layer 2. The P well regions 3, 30, 31 shown in the drawing are independent of and isolated from one another.

P^+ regions 300 and 310 are shallower than the P well regions 30 and 31, and self-aligned with a gate electrode 9 consisting of a polycrystalline semiconductor

or so-called polycrystalline silicon inside the P well regions 30 and 31, respectively. An N^+ region 5 is formed self-aligned with respect to the gate electrode 9 inside the P^+ regions 300 and 310. This N^+ region 5 serves as the source region of the MOSFET. A source electrode S consisting of a metal such as aluminum is connected to the N^+ region 5 and to the P^+ regions 300 and 310 via through-holes of an inter-layer insulating film such as a phosphosilicate glass film 10.

The surfaces of the P^+ regions 300 and 310 form an N channel layer which connects the N^- semiconductor layer (drain region) 2 to the N^+ region (source region) 5 by a voltage applied to its gate electrode 9. In other words, the vertical MOSFET is fundamentally composed of the N^- semiconductor layer 2, the P^+ regions 300, 310, the N^+ region 5, the gate insulating film 7 and the gate electrode 9.

The P well regions 30 and 31 are formed in order to improve the withstand voltage (drain withstand voltage) of the P-N junctions between the N^- semiconductor layer 2 and the P^+ region 300 and between the N^- semiconductor layer 2 and the P^+ region 310, respectively. The P^+ regions 300, 310 are one of the factors that determine the channel length (distance between the drain and source) and are formed with a reduced thickness so as to reduce the channel length. For this reason, the cylindrical portion of the above-mentioned P-N junction is likely to cause electric field concentration and be broken down by a low voltage. To prevent this breakdown, the P well regions 30 and 31, which are deeper than the P^+ regions 300 and 310, are provided to mitigate the electric field concentration upon the cylindrical portion of the P-N junction.

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A P contact region 4 is selectively formed inside the P well region 3. This P^+ contact region is formed simultaneously with the formation of the P^+ regions 300 and 310. The source electrode S is connected to this P^+ contact region 4. The source electrode is formed so as to extend beyond the P well region 3 on the left side and to improve the withstand voltage of the P-N junction between the N^- semiconductor layer 2 and the P well region 3. A field insulating film (field SiO_2 film) 6 is formed on the surface of the P well region 3 and a polycrystalline semiconductor (polycrystalline silicon) layer 8 to be used as the protective element is formed on the surface of the field insulating film 6. As can be seen clearly from the drawing, this polycrystalline silicon layer 8 is formed continuous with gate electrode 9. The polycrystalline semiconductor layer 8 to function as the protective element consists of N^+ semiconductor portions 8a, 8b and a P semiconductor portion 8c interposed between these N^+ semiconductor portions 8a and 8b. The P-N junctions defined between the N^+ semiconductor portion 8a and the P semiconductor portion 8c and between the N^+ semiconductor portion 8b and the P semiconductor portion 8c together form the protective element of the MOSFET. That is to say, the polycrystalline semiconductor layer 8 forms a back-to-back diode. The P semiconductor portion 8c is converted into P type by doping with boron impurity when the P^+ regions 300, 310 and the P^+ contact region 4 are formed by doping with the boron impurity. This doping can be effected by ion implantation, for example. The ion implantation energy is about 75 KeV and the ion dose is about 8×10^{13} atoms/cm^2 in this case. On the other hand, the N^+ semiconductor portions 8a and 8b are converted into the N type by doping with a P impurity when the N^+ region (source region)

5 is formed by doping with P impurity. The doping can be done by ion implantation. The ion implantation energy is about 40 KeV and the ion dose is about 1.4×10^{16} atoms/cm^2 in this case. The source electrode S is connected to the N^+ semiconductor portion 8a via a through-hole of the phosphosilicate glass film 10. The gate electrode G is connected to the N^+ semiconductor portion 8b through a through-hole of the phosphosilicate glass film 10. The gate electrode G is made of a metallic material such as aluminum in the same way as the source electrode S. On the other hand, the drain electrode D made of a metallic material such as aluminum or nickel is formed on the back surface of the N^+ semiconductor substrate 1.

An N^+ region 50 and a guard ring electrode GR form a channel stopper (means for restricting the parasitic channel formed on the surface of the N^- semiconductor layer 2). This N^+ region 50 is formed simultaneously with the formation of the N^+ region 5. The P^+ region 40 is a scribe region which does not affect the characteristics of the MOSFET. The scribe region is a portion in which lines are scribed to divide the semiconductor wafer into a plurality of semiconductor pellets. It is necessary that the field insulating film be completely removed from the surface of the scribe region to facilitate scribing. It is further preferred that this field insulating film be removed without increasing the number of fabrication steps. The present embodiment takes this requirement into consideration. Namely, the scribe region in this embodiment is masked in the same step as the source contact portion. Accordingly, a P^+ region 40 having the same thickness as the P^+ contact region 4 and P^+ regions 300, 310 is formed inside the N^- semiconductor layer 2.

In this embodiment, the dimension of each layer

(or each film) is as follows:

N^- semiconductor layer 2	specific resistivity 20Ω·cm, 35 μm thick,
P well regions 3, 30, 31	10 μm deep,
P^+ regions 40, 300, 310, P^+ contact region	5 μm thick,
N^+ regions 5, 50	1 μm thick,
field insulating film 6	1.2 μm —1.5 μm thick,
gate insulating film 7	0.12 μm thick,
polycrystalline semiconductor layer 8, gate electrode 9	0.45 μm thick,
phosphosilicate glass film 10	0.5 μm thick,
source electrode S, gate electrode G, guard ring electrode GR	4.0 μm thick.

The vertical MOSFET shown in Figure 1 has an equivalent circuit shown in Figure 2. In this drawing, PD represents a back-to-back diode functioning as the protective element. This back-to-back diode PD consists of the polycrystalline semiconductor layer 8 shown in Figure 1. The diode D_1 in the back-to-back diode PD consists of the N^+ semiconductor portion 8b and the P semiconductor portion 8c of Figure 1 while diode D_2 is formed by the P semiconductor portion 8c and the N^+ semiconductor portion 8a of Figure 1.

The protective element shown in Figure 1, or the polycrystalline semiconductor layer 8 (8a, 8b, 8c) and the gate electrode (polycrystalline semiconductor) layer 9 are formed on the surface of a semiconductor pellet 100 as shown in Figure 3. In this drawing, the gate electrode 9 is shown formed in a mesh like a honeycomb H inside the entire frame represented by dotted lines. The polycrystalline semiconductor layer 8

is formed around the semiconductor pellet 100 encompassing this gate electrode 9.

The gate, source and guard ring electrodes G, S and GR are formed on the surface of the semiconductor pellet 100 on which the above mentioned polycrystalline semiconductor layer 8 and the gate electrode 9 are formed, as shown in Figure 4. Symbols GP and SP in Figure 4 represent respective bonding pad extensions of the gate electrode and the source electrode, to which wires are connected. To improve bondability, no polycrystalline semiconductor layer is formed immediately below these bonding pads GP and SP as is obvious from Figure 3.

The protective element will now be explained in detail with reference to Figures 5 and 6.

Figure 5 is an enlarged sectional view of the protective element (polycrystalline semiconductor layer 8) shown in Figure 1. In this drawing, the withstand voltage of each of the diodes D_1 and D_2 is determined by the P semiconductor portion 8c, so that the quantity of the impurity (doping quantity of B impurity) for forming this P semiconductor portion 8c is important. The following points were clarified in experiments carried out by the inventors of the present invention.

When the impurity dose is below 10^{13} atoms/cm^2, the diodes D_1, D_2 have a large series resistance and the withstand voltage of each of these diodes D_1, D_2 is determined by the punch-through phenomenon. Hence, the breakdown withstand current drops significantly. The withstand voltage of each of the diodes D_1, D_2 depends upon the machining accuracy and its variance is great. Accordingly this impurity dose quanitity (below 10^{13} atoms/cm^2) is not practical. On the other hand, if the impurity dose is above 10^{15} atoms/cm^2, not only is the withstand voltage of each

diode lowered but the leakage current also increases. Hence, this value is not practical either.

For the above mentioned reasons, the most preferred range of the impurity dose is from 10^{13} to 10^{15} atoms/cm^2. The impurity concentration of the P semiconductor portion 8c obtained by an impurity dose within this range was found to be 10^{17} to 10^{19} atoms/cm^3. This impurity dose is substantially in agreement with that when the P^+ regions 300 and 310 of the MOSFET are formed. Accordingly, the P semiconductor portion 8c can be formed simultaneously with the P^+ regions 300 and 310. Incidentally, the impurity dose for forming the N^+ semiconductor portions 8a, 8b was 10^{15} atoms/cm^2 (impurity concentration 2.5×10^{19} atoms/cm^3) or more.

In this embodiment, the impurity dose was 8×10^{13} atoms/cm^2 in the P semiconductor portion 8c and 1.4×10^{16} atoms/cm^2 in the N^+ semiconductor portions 8a and 8b, as described above. When the current-voltage characteristics between the electrode S and the electrode G in this case were measured, as shown in Fig. 6, it was found that the waveform in the forward direction F was symmetric to that in the reverse direction R about the origin as the centre, and the withstand voltage was $\pm$ 18V. Thus, the protective element in this embodiment sufficiently protects the MOSFET.

As can be seen clearly from Figures 1, 3 and 5, the protective element is not formed inside the semiconductor substrate but on the insulating film. Accordingly, reliability of the vertical MOSFET in this embodiment is higher since no thyrister operation occurs.

Furthermore, this embodiment provides the following effects:

(1) As can be understood more clearly from Figure 7, the protective element and the gate electrode of the

MOSFET in this embodiment are formed integrally with each other by the polycrystalline semiconductor layer. Accordingly, specific means for connecting the protective element to the gate electrode are eliminated and the semiconductor chip area is not increased. As can also be seen from Figure 7, the P-N junctions J_1 and J_2 are formed in a ring-like shape and the cross section of the junctions is not exposed. Hence, degradation of the characteristics of the protective element can be prevented.

(2) The protective element consisting of the polycrystalline semiconductor layers is formed on the insulating film (field insulating film 6) which is thicker than the gate insulating film (SiO_2) so that the influence of the field effect due to the drain voltage upon the protective element can be eliminated. Hence, the resulting protective element is mere reliable.

If the protective element were formed on a thin insulating film such as the gate insulating film, it would be influenced by the voltage (drain voltage) applied to the N^- semiconductor layer 2. In other words, the protective element itself would operate as a reverse MOSFET and lose its function of protecting the gate insulating film of the MOSFET. In accordance with this embodiment, however, the influence of the field effect due to the drain voltage can be reduced because the protective element is formed on the thick field insulating film.

(3) A sufficiently thick insulating film (field insulating film 6) thicker than the gate insulating film is formed between the end portion of the protective element consisting of the polycrystalline semiconductor layers (P semiconductor portion T shown in Figure 1) and the P^- semiconductor layer. Hence, the insulating film itself does not undergo dielectric breakdown.

(4) Because of the P well region 3 shown in Figure 1, the parasitic capacitance between the gate electrode G and the drain electrode D formed on the other main surface (back surface) of the semiconductor substrate 1 can be reduced.

If this P well region 3 were not provided, a large parasitic capacitance would exist between the gate electrode G and the drain electrode D across the field insulating film 6 and the gate insulating film 7. On the other hand, because of the P well region 3 connected to the source electrode S, there is substantially no parasitic capacitance across the field insulating film 6 and the gate insulating film 7 between the gate electrode G and the drain electrode D. Hence, the electric characteristics of the MOSFET are improved by the existence of this P well region 3.

(5) In addition, the provision of the P well region 3, further reduces the influence of the field effect due to the drain voltage upon the protective element.

The vertical MOSFET described in the above-mentioned embodiment can be fabricated in accordance with the following fabrication method with reference to Figures 8a through 8h.

(a) An N^- type Si layer 2 is formed by epitaxial growth on an N^+ type Si substrate 1 (see Figure 8a).

(b) An oxide film (SiO_2) 6 is formed by thermal oxidation of the surface and selective etching is effected to leave the field portion. Using the oxide film (field oxide film) 6 as a mask, boron ions are deeply implanted to form the P well regions 3, 30. After ion implantation, thermal oxide films (SiO_2) 6a and 6b are formed on the surface of the P well regions 30, 3 for the expansion diffusion treatment (see Figure 8b).

(c) The oxide films 6, 6a are selectively removed in order to expose part of the N^- type Si layer 2

and part of the P well region 30 on which the gate oxide film is to be formed. At the same time, the oxide film 6b on the P well region 3 is selectively removed to form a P^+ contact region while the oxide film 6 on the P^- type Si layer 2 is selectively removed to form an N^+ region (channel stopper) (see Figure 8c).

(d) Thin oxide films 7, 7a and 7b are formed on the surfaces of the exposed P well regions 3, 30 and P^- Si layer 2 by thermal oxidation (see Figure 8d). Only oxide film 7 serves as the gate oxide film of the MOSFET.

(e) Si is vapor-deposited on the surfaces of the oxide films 6, 7, 7a and 7b to form a polycrystalline Si layer, which is then selectively removed to form the polycrystalline Si layer 8 serving as the gate electrode 9 and protective element (see Figure 8e).

(f) Using the polycrystalline Si layers 8 and 9 as a mask, boron implantation and expansion diffusion are then carried out to form the P^+ region 300 which is thinner than the well region and is to serve as the channel portion of the MOSFET. In this case, boron is also introduced into the polycrystalline Si layers 8 and 9 and they are converted into the P type. Boron is also implanted into the P well region 3 through the thin oxide film 7a, thereby forming the P^+ contact region 4 (see Figure 8f). Incidentally, a photoresist film PF should be deposited on the thin oxide film 7b lest boron be implanted into the N^- Si layer 2 below the thin oxide film 7b.

(g) The oxide films 7, 7b are selectively removed using a photoresist film 11 and the polycrystalline Si layer 9 as a mask to expose the P^+ region 300 and the N^- Si layer 2. Phosphorous is ion-implanted into the surfaces of the P^+ region 300 and the thus

exposed N^- Si layer 2, and expansion diffusion is then carried out to form the N^+ region 5 (see Figure 8g). In this manner, the MOSFET is formed by double diffusion self-alignment. In this process, phosphorus is also introduced into the polycrystalline Si layers 8, 9, forming the N^+ semiconductor portions 8a, 8b and 9. Thus, a protective element having an NPN structure is obtained. In this process, too, the N^+ region 50 for the channel stopper is simultaneously formed inside the N^- Si layer 2.

(h) PSG (phosphosilicate glass) 10 is deposited on the entire surface of the N^- Si layer 2 and the PSG film 10 is then contact photo-etched. After evaporation of aluminum, the aluminum layer is pattern etched to form the source electrode S, the gate electrode G and the guard ring electrode GR (see Figure 8h).

The vertical MOSFET having the protective element is completed in the abovementioned manner.

The method for fabricating the MOSFET of the present invention described above provides the advantage in that no specific extra fabrication step is necessary to form the protective element.

In the abovementioned fabrication method, it is desirable to form thin oxide films on the surfaces of the polycrystalline Si layers 8 and 9 by oxidizing their surfaces before depositing the PSG film 10. Figure 9 is an enlarged sectional view of a protective element having such a thin oxide film. As the thin oxide film (SiO_2 film) 13 covers the P-N junctions J_1 and J_2 of the protective element and their end portions, leakage current and degradation of the withstand voltage and electrical characteristics of the protective element can be prevented.

Though the abovementioned method has been described with reference to the case in which the entire surface of the polycrystalline Si layer 8 is doped with boron

simultaneously with the formation of the channel portion (see Figure 8(f)), boron may be introduced to the polycrystalline Si layer 8 by forming a photoresist film 14 on the surface of the polycrystalline Si layer 8 as shown in Figure 10 and then partially introducing boron to form the P semiconductor portion 8c. This method helps to give the N^+ semiconductor portions 8a and 8b a sufficiently low resistance.

Examples of modifications of the protective element in accordance with the present invention will now be described.

Modification Example 1

The opposition length of the P-N junction is preferably elongated in order to obtain current capacitance when the protective element breaks down. To accomplish this object, the P-N junctions J_1, J_2 in the polycrystalline Si layer are folded in a sinuous or concertina fashion as shown in Figure 11. This arrangement enlarges the opposing area of the P-N junctions, stabilizes the diode withstand voltage and improves the gate protecting effect. The opposing line of the P-N junction can be folded not only in the case of the ring-like junction section but also in the case of an open junction section such as a straight line section.

Modification Example 2

In the foregoing description of the embodiment, the protective element using the polycrystalline Si layer forms two P-N junction diodes with reference to an example in which a P-N-P junction is formed. However, the present invention is not particularly limited to this structure. For example, the N^+ semiconductor portions 8a, 8d, 8b and the P semiconductor portions 8c, 8e are alternately formed on the polycrystalline Si layer 8, which is formed on the

insulating film 6, by selectively doping N and P impurities so as to form a protective element having an $N^+ - P - N^+ - P - N^+$ structure as shown in Figure 12. Figure 13 is a perspective view of the protective element having an $N^+ - P - N^+ - P - N^+$ structure and the gate electrode of the MOSFET, and Figure 14 is an equivalent circuit diagram of the MOSFET having the protective element of the $N^+ - P - N^+ - P - N^+$ structure.

All the foregoing embodiments deal with an N channel vertical MOSFET but the present invention is not limited to such a structure and can also be applied to a P channel vertical MOSFET. In the case of a P channel vertical MOSFET, all the conductivity types of the foregoing embodiments become the opposite but the basic structure remains the same as that of the N channel vertical MOSFET.

CLAIMS:

1. An insulated gate semiconductor device having an insulated gate field effect transistor forming part of a substrate and a protective element for protecting the gate electrode of the transistor, the protective element and the gate electrode being semiconductor layers integral with each other on an insulating film on the surface of the substrate, the part of the insulating film separating the semiconductor layer of the protective element from the substrate being thicker than the part of the insulating film separating the semiconductor layer of the gate electrode from the substrate.

2. A device according to claim 1, wherein the semiconductor layer of the protective element has one or more P-N junctions formed therein.

3. An insulated gate semiconductor device according to claim 2 wherein the P-N junction or junctions of the semiconductor layer of the protective element are shaped in such a manner that their cross-sections are not exposed.

4. A device according to any one of claims 1 to 3, wherein the transistor has a drain region of a first conductivity type, a channel region of a second conductivity type in the drain region, and a source region of the first conductivity type in the channel region.

5. An insulated gate semiconductor device according to claim 4, wherein another region of the second conductivity type is formed in the semiconductor substrate immediately below the semiconductor layer of the protective element and is electrically connected to the source region of the transistor.

6. An insulated gate semiconductor device substantially as herein described with reference to and as illustrated in Figs. 1 to 8 or Fig. 9, or Fig. 10, or those Figs. as modified by Fig. 11 or Fig. 12, or Figs. 13 and 14 of the accompanying drawings.

7. A method of fabricating an insulated gate semiconductor device including:

forming an insulated gate field effect transistor in a substrate,

forming an insulating film on a surface of the substrate, the insulating film having a first part and a second part thicker than the first part, and

forming integral semiconductor layers on the insulating film, the semiconductor layer on the thinner part of the insulating film being located relative to the transistor such that it forms a gate electrode, the semiconductor layer on the thicker part of the insulating film forming a protective device for protecting the gate electrode of the transistor.

8. A method according to claim 7, wherein the formation of the transistor includes:

introducing an impurity of a second conductivity type into the substrate using a part of the semiconductor layer on the thinner part of the insulating film as a mask, the substrate being of a first conductivity type, to form a channel region in parts of the substrate forming a drain region; and

introducing an impurity of the first conductivity type into the channel region, using a part of the semiconductor layer on the thinner part of the insulating film as a mask, to form a source region in the channel region.

9. A method according to claim 8, wherein the dose of impurity of the second conductivity type is between 10^{13} atoms/cm^2 and 10^{15} atoms/cm^2.

10. A method according to any one of claims 7 to 9, wherein an impurity of the or a first conductivity type is selectively introduced into the semiconductor layer on the thicker part of the insulating film, to form at least one P-N junction.

11. A method of fabricating an insulated gate semiconductor device substantially as any one herein described with reference to the accompanying drawings.