What is claimed is:

1. A capacitor, characterized by comprising an upper electrode, a lower electrode and a dielectric layer disposed between the upper electrode and the lower electrode, characterized in that, each of the upper electrode and the lower electrode comprises a metal layer, and the metal layer of the upper electrode and the metal layer of the lower electrode are made of a same material;

the capacitor is a trench capacitor including a substrate, and the substrate has a trench; and the upper electrode, the dielectric layer, and the lower electrode are formed on and cover a surface, on which the trench is located, of the substrate.

2. The capacitor according to claim 1, characterized in that, a material of the metal layers comprises Al, Au, Ti, or Cu.

3. The capacitor according to claim 1 or 2, characterized in that, both the upper electrode and the lower electrode are prepared by a physical vapor deposition process.

4. The capacitor according to claim 2, characterized in that, both a thickness of the upper electrode and a thickness of the lower electrode is in a range of 50nm to 500nm.

5. The capacitor according to claim 4, characterized in that, both the thickness of the upper electrode and the thickness of the lower electrode are in a range of 100nm to 300nm.

6. The capacitor according to claim 1, characterized in that, the dielectric layer comprises an Al_2O_3 layer, a TiO_2 layer, or an HfO_4 layer.

7. The capacitor according to claim 6, characterized in that, a thickness of the dielectric layer is in a range of 5nm to 15nm.

8. The capacitor according to claim 1, characterized in that, the capacitor is a high-density capacitor.

9. Semiconductor equipment, characterized in that, the semiconductor equipment is configured to manufacture the capacitor according to any one of claims 1 to 8, and comprises: a physical vapor deposition chamber, an atomic layer deposition chamber and a transport platform;

the physical vapor deposition chamber is configured to prepare the upper electrode and the lower electrode of the capacitor;

the atomic layer deposition chamber is configured to prepare the dielectric layer of the capacitor; and

the transport platform is respectively connected with the physical vapor deposition chamber and the atomic layer deposition chamber and is configured to transport a substrate.

10. The semiconductor equipment according to claim 9, characterized by further comprising a degas chamber configured to degas and anneal the substrate and connected with the transport platform.

11. The semiconductor equipment according to claim 9, characterized by further comprising a pre-clean chamber configured to remove impurities from a surface of the substrate and connected with the transport platform.

12. The semiconductor equipment according to claim 9, characterized in that, the semiconductor equipment comprises a plurality of physical vapor deposition chambers configured to deposit thin films of a plurality of materials, respectively.

13. The semiconductor equipment according to claim 9, characterized in that, a target-base distance is greater than 90mm in the physical vapor deposition chamber.

14. The semiconductor equipment according to claim 13, characterized in that, the target-base distance is in a range of 200mm to 410mm.

15. A manufacturing method of a capacitor, characterized by comprising:

forming a lower electrode on a surface, on which deposition is to be performed, of a substrate by a physical vapor deposition process;

forming a dielectric layer on a surface of the lower electrode away from the substrate by an atomic layer deposition process; and

forming an upper electrode on a surface of the dielectric layer away from the lower electrode by a physical vapor deposition process;

wherein each of the upper electrode and the lower electrode comprises a metal layer, and the metal layer of the upper electrode and the metal layer of the lower electrode are made of a same material.

16. The manufacturing method of a capacitor according to claim 15, characterized in that, a material of the metal layers comprises Al, Au, Ti, or Cu.

17. The manufacturing method of a capacitor according to claim 15, characterized in that, in the step of forming the upper electrode on the surface of the dielectric layer away from the lower electrode by the physical vapor deposition process, a process pressure is in a range of 0mTorr to 2mTorr, a sputtering power is in a range of 30kW to 38kW, and a bias power is in a range of 400W to 1000W.

18. The manufacturing method of a capacitor according to claim 15, characterized in that, the dielectric layer comprises an Al_2O_3 layer, a TiO_2 layer, or an HfO_4 layer.

19. The manufacturing method of a capacitor according to claim 15, characterized in that, a process temperature is in a range of 300°C to 400°C in the step of forming the dielectric layer on the surface of the lower electrode away from the substrate by the atomic layer

deposition process.

20. The manufacturing method of a capacitor according to claim 15, characterized by further comprising a degassing process for degassing the surface, on which deposition is to performed, of the substrate before the step of forming the lower electrode on the surface, on which deposition is to performed, of the substrate by the physical vapor deposition process.

21. The manufacturing method of a capacitor according to claim 15, characterized by further comprising an annealing process after the step of forming the upper electrode on the surface of the dielectric layer away from the lower electrode by the physical vapor deposition process.