

Description

The invention relates to an arrangement for generating a frequency control signal that is coupled to a controlled oscillator, used in, for example, a stereo decoder of a television apparatus.

Typical baseband composite audio stereo signals include a main signal formed from the sum of the left and right channel signals (L+R), a pilot signal having a frequency ω_p which is greater than the maximum frequency of the (L+R) signal, and a difference signal (L-R) which is the difference between the left and right channel signals. The difference signal is in the form of a double sideband, amplitude modulated suppressed carrier centered at a frequency of twice ω_p . The pilot signal is essential for demodulating the suppressed carrier to extract the (L-R) audio information.

The demodulated (L-R) signal will nominally include a component corresponding to the pilot signal, and the maximum signal frequency of the (L+R) signal is nominally relatively close to the pilot signal frequency.

In such stereo decoder, a phase-lock-loop circuit (PLL) may be used for generating, for example, a signal at the frequency $2\omega_p$ that is synchronized to the pilot signal and that is used for demodulating the (L-R) signal.

U.S. Patent Application US-A-4 731 844 published 15.03.88 after the priority date of the present application, and entitled, APPARATUS FOR CANCELLING A PILOT SIGNAL FROM A COMPOSITE SIGNAL, in the name of Todd Christopher describes a stereo decoder in which the baseband composite audio stereo signals are sampled for producing a digital signal comprising sequentially provided digital words. A PLL that demodulates the (L-R) signal includes a voltage-controlled crystal oscillator (VCXO). An output signal of the VCXO is at a frequency that is equal, for example, to an integer multiple of the pilot signal. A phase or frequency error signal that is indicative of a corresponding phase or frequency error of the VCXO output signal relative to that of the pilot signal is generated. The frequency error signal in, for example, the Todd arrangement is represented by a digital word.

It may be desirable to generate from the digital frequency error signal, an analog frequency control signal that is to be applied to a frequency control terminal of the VCXO for controlling the frequency and phase of the VCXO output signal.

In carrying out an aspect of the invention, in a stereo decoder apparatus that is responsive to a baseband composite audio signal that includes a pilot signal component a controllable oscillator responsive to a first control signal is included. The oscillator generates an oscillatory signal at a fre-

quency that is controlled in accordance with the first control signal. A phase error indicative signal that forms a digital word having a value that is indicative of a phase difference between the pilot signal component and the oscillatory signal is generated. A first current is coupled to a capacitance for a given interval. A second control signal is generated for varying the duration of the given interval in which the first current is coupled to the capacitance so as to develop the first control signal in the capacitance.

FIGURE 1 illustrates a block diagram of a portion of a stereo decoder that includes a charge pump arrangement, embodying an aspect of the invention, for controlling the frequency of a voltage controlled crystal oscillator; and

FIGURE 2 illustrates a detailed embodiment of the charge pump arrangement of FIGURE 1, embodying an aspect of the invention.

In FIGURE 1, a composite audio stereo signal IN_a that is obtained from, for example, an FM decoder of a television receiver, not shown in the figures, is coupled to an input terminal 109a of an analog-to-digital converter 109 that generates a composite signal IN_b . Signal IN_b is a digital representation of a signal having a frequency composition similar to the spectral waveform 5 that contains a pilot signal component PILOT. Signal component PILOT is, in the BTSC standard, at a frequency ω_p that is equal to the horizontal scan frequency, f_H .

Signal IN_b is applied via a conductor 110 to the minuend input terminal of a signal subtraction circuit 112 of a phase-lock-loop circuit (PLL) 100. A synthesized pilot signal P_s is coupled via connection 111 to the subtrahend input terminal of subtraction circuit 112. Subtraction circuit 112 provides a composite signal 112a, with the pilot signal component substantially eliminated, at its output connection 113. Subtraction circuit 112 is included in a circuit 99 shown within the dashed-line. Circuit 99 performs the analogous function of a phase detector in a conventional PLL.

Signal 112a is also coupled to a low-pass filter 115 which passes, or separates the (L+R) signal to the substantial exclusion of higher frequency components of the composite signal. Since the pilot signal component is not present in the signal applied to filter 115, the frequency cut off characteristics of filter 115 are, advantageously, significantly less critical than if the pilot signal component were present.

Output signal 112a from subtraction circuit 112 is, additionally, coupled to one input of a multiplier circuit 120 that is included in circuit 99. The output developed by the multiplier 120 is coupled to serially coupled circuit elements including a low pass filter 122, a charge pump arrangement 123, embodying an aspect of the invention, a voltage con-

trolled crystal oscillator (VCXO) 124, a sinewave generator circuit 126 and a 90° phase shifter 128.

Low-pass filter 122, of unit 1222, having a cutoff frequency that is substantially lower than that of pilot signal component PILOT, low-pass filters the digital output words at a port 120a of multiplier 120 to produce an error word 122b that is representative of a phase or of a frequency error between signal component PILOT and an output signal CK of VCXO 124, as described later on. Digital error word 122b is then periodically applied every, for example, 2/3 of the period of pilot signal component PILOT, to charge pump arrangement 123, embodying an aspect of the invention, to produce an equivalent analog signal 123a, that remains substantially constant between the above-mentioned periodic application intervals. Signal 123a is coupled to an input terminal of VCXO 124 to establish the output frequency produced thereby.

For a zero average value of the signal at port 120a of multiplier 120, VCXO 124 develops output signal CK having a frequency that is substantially equal to a predetermined integer multiple N of the frequency, ω_p , of pilot signal component PILOT.

Output signal CK from VCXO 124 is applied to sinewave generator 126 which develops a signal 126a that provides a digital representation of a sinusoidal signal, $\sin(\omega_p't)$, that is in the same frequency and in the same phase as pilot signal component PILOT. Sinewave generator 126 may include, for example, a counter that counts pulses of signal CK and a read-only-memory (ROM), having an address port that is coupled to an output word of the counter, such that signal 126a is produced at an output port of such ROM. Generator 126 establishes the value of integer N that was mentioned before, to be equal, for example, to 700, in accordance with the ratio between the frequency of signal CK and that of signal 126a generated by generator 126. Output signal 126a of sinewave generator 126 is coupled to phase shifter 128 which develops, in a well known manner, a cosine signal of at the same frequency of, but in a phase that is shifted by 90°, which signal corresponds to the expression $\cos(\omega_p't)$.

Standard FM and BTSC baseband composite audio signals, $C(t)$, can be described by the equation

$$C(t) = S(t) + P\sin(\omega_p t) + D(t)\sin(2\omega_p t) \quad (1)$$

where $C(t)$ corresponds to signal IN_D , and $S(t)$ and $D(t)$ correspond to the time varying (L+R) and (L-R) signals respectively, P is the amplitude, and ω_p the radian frequency of pilot signal component PILOT.

Synthesized pilot signal P_s , applied to subtraction circuit 112, is developed by measuring the

amplitude of the residual pilot signal at the output of subtraction circuit 112, effectively amplifying the residual amplitude, and multiplying this value by the output of sinewave generator 126.

Assume that the amplitude, P_s , of synthesized pilot signal P_s exactly equals the amplitude P of pilot signal component PILOT. Also, the synthesized pilot signal P_s can be represented as $P_s\sin(\omega_p't)$. The value $C(t)$ obtained from subtraction circuit 112 that is representative of signal 112a may be expressed as

$$C(t) = S(t) + P\sin(\omega_p t) - P_s\sin(\omega_p't) + D(t)\sin(2\omega_p t) \quad (2)$$

The value $C(t)$ is multiplied in multiplier 120 by $\cos(\omega_p't)$ to yield

$$C(t)\cos(\omega_p't) = S(t)\cos(\omega_p't) + P\sin(\omega_p t)\cos(\omega_p't) - P_s\sin(\omega_p't)\cos(\omega_p't) + D(t)\sin(2\omega_p t)\cos(\omega_p't) \quad (3)$$

The first and last terms in equation (3) are sinusoids which will average to zero in the low-pass filter 122. The center two terms, $P\sin(\omega_p t)\cos(\omega_p't) - P_s\sin(\omega_p't)\cos(\omega_p't)$, may be shown, by manipulating trigonometric identities, to be equivalent to

$$P/2(\sin(\omega_p t - \omega_p't) + \sin(\omega_p t + \omega_p't) - \sin(2\omega_p't)) \quad (4)$$

The two rightmost terms are relatively high frequency sinusoids and will average to zero in the low-pass filter 122. Since the nominal output frequency of signal 126a of sinewave generator 126 is established close to ω_p , the argument $(\omega_p t - \omega_p't)$ of the first term of expression (4) will be close to zero. The term $\sin(\omega_p t - \omega_p't)$ will be a very low frequency sinusoid and will not average to zero unless ω_p' equals ω_p . Therefore, as long as the frequency ω_p' is different from the pilot frequency ω_p , multiplier 120 and low-pass filter 122 will periodically vary error signal 122b that is applied to VCXO 124 in a negative feedback manner that will tend to synchronize signal 126a of sinewave generator 126 to pilot signal component PILOT.

Next, consider, for example, that ω_p' and ω_p are identical frequencies but that synthesized pilot signal P_s and pilot signal component PILOT are out of phase by Δ degrees. In this instance, the output of multiplier 120 takes the form

$$C(t)\cos(\omega_p't + \Delta) = S(t)\cos(\omega_p't + \Delta) + P\sin(\omega_p t)\cos(\omega_p't + \Delta) - P_s\sin(\omega_p't + \Delta)\cos(\omega_p't + \Delta) + D(t)\sin(2\omega_p t)\cos(\omega_p't + \Delta) \quad (5)$$

The first and fourth terms on the right hand side of equation will average to zero in low-pass filter 122 since they represent sinusoidal signals having frequencies relatively high compared to the

reciprocal time constant of the filter. The two middle terms can be shown to be equivalent to

$$P/2(\sin(2\omega_p t + \Delta) + \sin\Delta - \sin(2\omega_p t + 2\Delta)). \quad (6)$$

The first and third terms are relatively high frequency sinusoidal signals and will average to zero in low-pass filter 122 of PLL 100. The remaining term, $P/2\sin\Delta$, is substantially a DC term and, thus, will be passed by the low-pass filter 122 to form error signal 122b that provides a phase correction term to VCXO 124. Thus, as long as a frequency or phase error exists, multiplier 120, low-pass filter 122 and charge pump arrangement 123 will vary signal 123a. If no error exists, signal 123a remains constant.

Signal CK is coupled to an input terminal of a sinewave generator 150 that generates a signal 150a that is a digital representation of a sinewave at the radian frequency $2\omega_p$. Sinewave signal 150a is coupled to a multiplicand input port of a multiplier 116. Composite signal IN_p , less the synthesized pilot signal P_s obtained from subtraction circuit 112, is coupled to respective multiplicand input terminals of multipliers 116 and 138. Signal 150a from sinewave generator 150, that varies in accordance with the expression $\sin(2\omega_p t)$, is applied to a multiplier input terminal of multiplier 116 to produce the signal (L-R), described by the equation

$$(L-R) = S(t)\sin(2\omega_p t) + D(t)\sin(2\omega_p t)\sin(2\omega_p t) \quad (7)$$

$$(L-R)' = S(t)\sin(2\omega_p t) + D(t)(1 - \cos^2(2\omega_p t)) \quad (8)$$

which is applied to a low-pass filter 118. Low-pass filter 118 is designed to pass only the baseband term $D(t)$, thus the (L-R) signal is separated.

The output from subtraction circuit 112 is multiplied by the term $\sin(\omega_p t)$ in multiplier 138. Therefore, output signal P_o of multiplier 138 may be expressed as

$$P_o = S(t)\sin(\omega_p t) + P_s\sin(\omega_p t)\sin(\omega_p t) - P_c\sin(\omega_p t)\sin(\omega_p t) + D(t)\sin(2\omega_p t)\sin(\omega_p t). \quad (9)$$

The term $P_c\sin(\omega_p t)\sin(\omega_p t)$ corresponds to the pilot cancelling signal, as described in detail in U.S. Patent Application No. 882,384 entitled APPARATUS FOR CANCELLING A PILOT SIGNAL FROM A COMPOSITE SIGNAL, in the name of Todd Christopher. Signal P_o is applied to a low-pass filter 132 which integrates the signal over a relatively long period compared to $2\pi/\omega_p$. An output signal of filter 132, applied to multiplier 134 is multiplied by signal 126a of generator 126 to generate synthesized pilot signal P_s .

FIGURE 2 illustrates charge pump arrangement 123 of FIGURE 1, embodying an aspect of the

invention, in more detail. Similar numbers and symbols in FIGURES 1 and 2 illustrate similar items or functions. Error word or signal 122b of FIGURE 1, that is represented, for example, as a 2's complement binary word, is coupled to an input port 200a of an absolute value forming stage 200 that generates a word 200b representing the absolute value of signal 122b. A sign bit of signal 122b is coupled to a data input terminal 201a of a flip-flop 201. Word 200b is coupled to preset input port 202a of a counter 202, operating as a count-down counter. A timing unit 203 generates a signal LOAD that occurs, periodically such as, for example, every interval that is equal to, for example, 2/3 of the period of pilot signal component PILOT of FIGURE 1. When signal LOAD of FIGURE 2 occurs, signal 200b is stored in counter 202 that causes counter 202 to be preset to the value of signal 200b. Simultaneously, the sign bit of signal 122b is stored separately in flip-flop 201. As a result of signal LOAD, an output signal 202b of counter 202 is initially equal to signal 200b. Signal 202b is coupled to an input port of a zero detector 207 that generates a signal NONZERO as long as signal 202b is nonzero. Signal NONZERO is coupled to enable terminal 202c of counter 202 that enables counter 202 to count down as long as signal NONZERO is generated. Consequently, counter 202 output signal 202b has a value that decreases sequentially from the initially preset value, each time signal CK generated by VCXO 124 occurs. When counter 202 output signal 202b becomes zero, generation of signal NONZERO ceases and counter 202 ceases counting down until the next time signal LOAD occurs.

Thus, signal NONZERO forms a pulse having a variable width, or duration W_1 that is indicative of the absolute value of digital signal 122b. The value of signal 122b is determined in accordance with the weighted value of the bits of each word of signal 122b. Signal NONZERO is coupled to an input terminal 204a of an AND gate 204 that receives a signal PLUS from an output terminal of flip-flop 201. Signal PLUS is generated when signal 122b is positive. Consequently, a variable width output pulse of a signal CHARGE, having the same duration as that of signal NONZERO, is generated when signal 122b is positive. On the other hand, a signal DISCHARGE that is similar to signal CHARGE is generated at an output terminal 205a of an AND gate 205 when signal NONZERO is generated, provided flip-flop 201 generates a signal MINUS that occurs when signal 122b is negative.

In accordance with a feature of the invention, signal CHARGE is coupled to the corresponding control terminals of analog switches ASW1 and ASW2 that causes switch ASW1 to couple a current i_b generated by a current source IS3 to a

capacitor C4 as indicated by the solid-line wiper arm positions of switches ASW1 and ASW2. Current i_3 causes capacitor C4 to charge only during the pulse duration W_1 of signal CHARGE. Source IS3 may be constructed in a conventional manner using MOS technology in a manner not shown in FIGURE 2.

In accordance with another feature of the invention, when current i_3 is not coupled to capacitor C4, that occurs outside the pulse duration W_1 , switch ASW2 couples current i_3 to voltage +VREF, as indicated by the dashed-line wiper arm positions of switches ASW1 and ASW2. In this way, current source IS3 supplies current i_3 continuously that prevents it from saturating or from operating in an undesirable mode of operation. Moreover, since the flow of current i_3 is uninterrupted by the switching operation of switch ASW1, current i_3 is, advantageously, at the desired level immediately after a leading edge LE of, for example, signal CHARGE occurs.

In a similar manner, signal DISCHARGE is coupled to control terminals of switches ASW3 and ASW4 that operate similarly to switches ASW1 and ASW2, respectively. Switch ASW3, as shown by the dashed line, couples a current i_4 produced by a current sink IS4, that is similar to current source IS3, to capacitor C4 for discharging capacitor C4 during a pulse duration W_2 of signal DISCHARGE. When switch ASW3 is conductive, switch ASW4 is nonconductive, and vice versa.

Thus, immediately after the generation of signal LOAD, capacitor C4 may be charged, if signal 122b is positive, it may be discharged, if signal 122b is negative or it may remain same if signal 122b is zero. The increase or decrease, respectively, in the level of signal 123a that is developed in capacitor C4 when signal 123 is, for example, positive is proportional to the value of error signal 122b. In this way, frequency control signal 123a is developed by means of the periodic accumulation of error signal 122b, in accordance with the periodic generation of signal LOAD. Frequency control signal 123a is coupled to the frequency control terminal of VCXO 124 of FIGURE 1 that generates signal CK at a frequency that is controlled by signal 123a.

An example of a circuit such as VCXO 124 having an MOS input transistor is described in detail in U.S. Patent Application serial number 091,167, entitled, A CONTROLLED OSCILLATOR in the name of P.D. Filliman, filed 31 August 1987.

VCXO 124 includes an input stage that is responsive to signal 123a. The input stage includes an MOS transistor 124c having a gate electrode that is coupled to a terminal 124b through which signal 123a is applied to VCXO 124. Because of the high input impedance at the gate of transistor

124c the charge of capacitor C4 of FIGURE 2 is substantially maintained the same during each interval that occurs when none of signal CHARGE and DISCHARGE is generated. In this way, the phase of VCXO 124 remains substantially stable when VCXO is phase-locked to pilot component signal PILOT of FIGURE 1.

Claims

1. A stereo decoder apparatus responsive to an analog composite signal containing audio information that includes a pilot signal component, comprising:

a controllable oscillator (124) responsive to an analog first control signal (123a), said oscillator generating an oscillatory signal at a frequency that is controlled in accordance with said first control signal; and characterized by

sampling means responsive to said analog composite signal for sampling said composite signal to generate therefrom bit weighted sampled signal having a first plurality of bits that represent said composite signal in a numerical, bit weighted form and that contains said synchronization information of said pilot signal component;

means (120) responsive to said sampled signal and to said oscillatory signal for generating a phase error indicative signal (122a) that forms a digital word having a second plurality of bits with a numerical bit weighted value that is indicative of a phase difference between said pilot signal component and said oscillatory signal;

a source (IS3) of a first current (i_3);

a capacitance (C4);

controllable

means

(204,205,ASW1,ASW2,ASW3,ASW4)) responsive to a second control signal that is coupled to a control terminal thereof for coupling said first current (i_3) to said capacitance for a given interval; and

means (200,202,203,204) responsive to said second plurality of bits of said phase error indicative signal for generating said second control signal in a manner that varies a length of said given interval in which said first current is coupled to said capacitance so as to develop said analog first control signal in said capacitance.

2. An apparatus according to Claim 1 characterized in that said second control signal generating means comprises a counter (202) that is preset in accordance with a value of said phase error indicative signal, wherein said counter (202) that is responsive to a clock

capacitor C4 as indicated by the solid-line wiper arm positions of switches ASW1 and ASW2. Current i_3 causes capacitor C4 to charge only during the pulse duration W_1 of signal CHARGE. Source IS3 may be constructed in a conventional manner using MOS technology in a manner not shown in FIGURE 2.

In accordance with another feature of the invention, when current i_3 is not coupled to capacitor C4, that occurs outside the pulse duration W_1 , switch ASW2 couples current i_3 to voltage +VREF, as indicated by the dashed-line wiper arm positions of switches ASW1 and ASW2. In this way, current source IS3 supplies current i_3 continuously that prevents it from saturating or from operating in an undesirable mode of operation. Moreover, since the flow of current i_3 is uninterrupted by the switching operation of switch ASW1, current i_3 is, advantageously, at the desired level immediately after a leading edge LE of, for example, signal CHARGE occurs.

In a similar manner, signal DISCHARGE is coupled to control terminals of switches ASW3 and ASW4 that operate similarly to switches ASW1 and ASW2, respectively. Switch ASW3, as shown by the dashed line, couples a current i_4 produced by a current sink IS4, that is similar to current source IS3, to capacitor C4 for discharging capacitor C4 during a pulse duration W_2 of signal DISCHARGE. When switch ASW3 is conductive, switch ASW4 is nonconductive, and vice versa.

Thus, immediately after the generation of signal LOAD, capacitor C4 may be charged, if signal 122b is positive, it may be discharged, if signal 122b is negative or it may remain same if signal 122b is zero. The increase or decrease, respectively, in the level of signal 123a that is developed in capacitor C4 when signal 123 is, for example, positive is proportional to the value of error signal 122b. In this way, frequency control signal 123a is developed by means of the periodic accumulation of error signal 122b, in accordance with the periodic generation of signal LOAD. Frequency control signal 123a is coupled to the frequency control terminal of VCXO 124 of FIGURE 1 that generates signal CK at a frequency that is controlled by signal 123a.

An example of a circuit such as VCXO 124 having an MOS input transistor is described in detail in U.S. Patent Application serial number 091,167, entitled, A CONTROLLED OSCILLATOR in the name of P.D. Filliman, filed 31 August 1987.

VCXO 124 includes an input stage that is responsive to signal 123a. The input stage includes an MOS transistor 124c having a gate electrode that is coupled to a terminal 124b through which signal 123a is applied to VCXO 124. Because of the high input impedance at the gate of transistor

124c the charge of capacitor C4 of FIGURE 2 is substantially maintained the same during each interval that occurs when none of signal CHARGE and DISCHARGE is generated. In this way, the phase of VCXO 124 remains substantially stable when VCXO is phase-locked to pilot component signal PILOT of FIGURE 1.

Claims

1. A stereo decoder apparatus responsive to an analog composite signal containing audio information that includes a pilot signal component, comprising:

a controllable oscillator (124) responsive to an analog first control signal (123a), said oscillator generating an oscillatory signal at a frequency that is controlled in accordance with said first control signal; and characterized by

sampling means responsive to said analog composite signal for sampling said composite signal to generate therefrom bit weighted sampled signal having a first plurality of bits that represent said composite signal in a numerical, bit weighted form and that contains said synchronization information of said pilot signal component;

means (120) responsive to said sampled signal and to said oscillatory signal for generating a phase error indicative signal (122a) that forms a digital word having a second plurality of bits with a numerical bit weighted value that is indicative of a phase difference between said pilot signal component and said oscillatory signal;

a source (IS3) of a first current (i_3);

a capacitance (C4);

controllable means (204,205,ASW1,ASW2,ASW3,ASW4) responsive to a second control signal that is coupled to a control terminal thereof for coupling said first current (i_3) to said capacitance for a given interval; and

means (200,202,203,204) responsive to said second plurality of bits of said phase error indicative signal for generating said second control signal in a manner that varies a length of said given interval in which said first current is coupled to said capacitance so as to develop said analog first control signal in said capacitance.

2. An apparatus according to Claim 1 characterized in that said second control signal generating means comprises a counter (202) that is preset in accordance with a value of said phase error indicative signal, wherein said counter (202) that is responsive to a clock



signal counts pulses of said clock signal during said given interval and wherein said second control signal is generated as long as said counter counts said pulses of said clock signal.

3. An apparatus according to Claim 1 characterized in that said second control signal is generated when said phase error indicative signal is at a first polarity (PLUS) and is not generated when said phase error indicative signal is at the opposite polarity.

4. An apparatus according to Claim 3 characterized in that said controllable means that couples said first current to said capacitor (C4) comprises a first switch (ASW1) that is conductive when said second control signal is generated.

5. An apparatus according to Claim 4 further characterized by, means (205) responsive to said phase error indicative signal for generating a third control signal (DISCHARGE) during a second given interval that varies in accordance with said value of said phase error indicative signal such that said third control signal is generated when said phase error indicative signal is at said opposite polarity, and a second switch that is conductive during said second given interval when said third control signal is generated for coupling a source (IS4) of a second current (I4) to said capacitor (C4) that changes said first control signal in said capacitor in an opposite manner to that of said first current (I3).

6. An apparatus according to Claim 5 further characterized by a third switch (ASW2) responsive to said second control signal that is conductive when said first switch (ASW1) is non-conductive, and vice versa, for forming an alternate current path to said first current (I3) when said first switch (ASW1) is nonconductive.

7. An apparatus according to Claim 6 characterized in that said third switch (ASW2) causes the flow of said first current to be substantially uninterrupted when said first switch (ASW1) changes from being conductive to being non-conductive and from being nonconductive to being conductive.

8. An apparatus according to Claim 1 characterized in that said controllable oscillator (124) includes an FET transistor (124c) having a gate electrode thereof coupled to said first control signal such that a high input impedance of said

FET transistor prevents a charge in said capacitance (C4) from changing outside said given interval.

9. An apparatus according to Claim 1 characterized in that said second control signal has a pulse duration that determines said length of said given interval when said first current is coupled to said capacitance.

10. An apparatus according to Claim 1 characterized in that said second control signal is generated only when a phase difference between said pilot signal component and said oscillatory signal is at a first polarity.

11. An apparatus according to Claim 1 characterized in that said controllable means comprises, means (200) for generating a second phase indicative signal forming a digital word having a value that is equal to an absolute value of said first phase error indicative signal for controlling the length of said given interval in accordance with said absolute value.

12. An apparatus according to Claim 1 further characterized by a source (IS4) of a second current (I4), wherein said controllable means couples said first current (I3) to said capacitance (C4) when said phase difference is at a first polarity and couples said second current (I4) to said capacitance when said phase difference is at the opposite polarity such that, during a given phase detection cycle, as long as said phase difference is at said first polarity, said second current (I4) is decoupled from said capacitance (C4) and, as long as said phase difference is at the opposite polarity, said first current (I3) is decoupled from said capacitance (C4).

Patentansprüche

1. Stereocodiereinrichtung, welche auf ein analoges Signalgemisch reagiert, das Audioinformation einschließlich eines Pilotsignalanteils enthält, mit:

einem steuerbaren Oszillator (124), der auf ein analoges erstes Steuersignal (123a) reagiert und ein Schwingungssignal mit einer Frequenz liefert, die entsprechend dem ersten Steuersignal gesteuert ist,

gekennzeichnet durch

eine auf das analoge Signalgemisch ansprechende Abgreifanordnung zum Abgreifen des Signalgemisches, um aus diesem ein bitgewichtetes abgegriffenes Signal zu erzeugen, welches eine erste Mehrzahl von Bits aufweist,



die das Signalgemisch in numerischer, bitgewichteter Form darstellen, und das die Synchronisierungsinformation des Pilotsignalanteiles enthält;

einer auf das abgegriffene Signal und das Schwingungssignal reagierende Anordnung (120) zum Erzeugen eines phasenfehleranzeigenden Signals (122a), welches ein digitales Wort mit einer zweiten Mehrzahl von Bits mit einem numerischen, bitgewichteten Wert bildet, der eine Phasendifferenz zwischen dem Pilotsignalanteil und dem Schwingungssignal anzeigt;

eine Quelle (IS3) für einen ersten Strom (i3);

eine Kapazität (C4);

eine steuerbare Anordnung (204, 205, ASW1, ASW2, ASW3, ASW4), die auf ein zweites Steuersignal, das auf einen Steueranschluß dieser Anordnung gekoppelt ist, anspricht, um den ersten Strom (i3) für ein gegebenes Intervall auf die Kapazität zu koppeln; und

eine Anordnung (200, 202, 203, 204), die auf die zweite Mehrzahl von Bits des phasenfehleranzeigenden Signals reagiert, um das genannte zweite Steuersignal in einer Weise zu erzeugen, daß die Länge des gegebenen Intervalles, in dem der erste Strom auf die Kapazität gekoppelt wird, verändert wird, um das analoge erste Steuersignal in der Kapazität zu bilden.

2. Einrichtung nach Anspruch 1, **dadurch gekennzeichnet**, daß die das zweite Steuersignal erzeugende Anordnung einen Zähler (202) enthält, der entsprechend einem Wert des phasenfehleranzeigenden Signals voreingestellt wird, wobei der Zähler, der auf ein Taktsignal reagiert, Impulse des Taktsignals während des gegebenen Intervalles zählt und wobei das zweite Steuersignal solange erzeugt wird, wie der Zähler die Impulse des Taktsignals zählt.
3. Einrichtung nach Anspruch 1, **dadurch gekennzeichnet**, daß das zweite Steuersignal erzeugt wird, wenn das phasenfehleranzeigende Signal eine erste Polarität (PLUS) hat und nicht erzeugt wird, wenn das phasenfehleranzeigende Signal die entgegengesetzte Polarität hat.
4. Einrichtung nach Anspruch 3, **dadurch gekennzeichnet**, daß die steuerbare Anordnung, die den ersten Strom auf den Kondensator (C4) koppelt, einen ersten Schalter (ASW1) enthält, der leitet, wenn das zweite Steuersignal erzeugt wird.

5. Einrichtung nach Anspruch 4, weiterhin **gekennzeichnet durch** eine Anordnung (205), die auf das phasenfehleranzeigende Signal reagiert, um ein drittes Steuersignal (ENTLADEN) während eines zweiten gegebenen Intervalles zu erzeugen, das entsprechend dem Wert des phasenfehleranzeigenden Signals so variiert, daß das dritte Steuersignal erzeugt wird, wenn das phasenfehleranzeigende Signal die entgegengesetzte Polarität hat, und durch einen zweiten Schalter, der während des zweiten gegebenen Intervalles leitet, wenn das dritte Steuersignal erzeugt wird, um eine Quelle (IS4) eines zweiten Stromes (i4) auf den Kondensator (C4) zu koppeln, der das erste Steuersignal am Kondensator in entgegengesetzter Weise wie der erste Strom (i3) ändert.

6. Einrichtung nach Anspruch 5, weiterhin **gekennzeichnet durch** einen dritten Schalter (ASW2), der auf das zweite Steuersignal anspricht und leitet, wenn der erste Schalter (ASW1) nicht leitet und umgekehrt, um einen alternativen Stromweg für den ersten Strom (i3) zu bilden, wenn der erste Schalter (ASW1) nicht leitend ist.

7. Einrichtung nach Anspruch 6, **dadurch gekennzeichnet**, daß der dritte Schalter (ASW2) bewirkt, daß der Fluß des ersten Stromes im wesentlichen nicht unterbrochen wird, wenn der erste Schalter (ASW1) von leitend auf nichtleitend und von nichtleitend auf leitend umschaltet.

8. Einrichtung nach Anspruch 1, **dadurch gekennzeichnet**, daß der steuerbare Oszillator (124) einen FET-Transistor (124c) enthält, der eine mit dem ersten Steuersignal gekoppelte Gateelektrode aufweist, so daß eine hohe Eingangsimpedanz des FET-Transistors verhindert, daß sich die Ladung der Kapazität (C4) außerhalb des gegebenen Intervalles ändert.

9. Einrichtung nach Anspruch 1, **dadurch gekennzeichnet**, daß das zweite Steuersignal eine Impulsdauer hat, welche die Länge des gegebenen Intervalles bestimmt, wenn der erste Strom auf die Kapazität gekoppelt wird.

10. Einrichtung nach Anspruch 1, **dadurch gekennzeichnet**, daß das zweite Steuersignal nur dann erzeugt wird, wenn die Phasendifferenz zwischen dem Pilotsignalanteil und dem Schwingungssignal eine erste Polarität hat.

11. Einrichtung nach Anspruch 1, **dadurch gekennzeichnet**, daß die steuerbare Anordnung



eine Vorrichtung (200) zum Erzeugen eines zweiten phasenfehleranzeigenden Signals aufweist, das ein Digitalwort mit einem Wert bildet, der gleich einem Absolutwert des ersten phasenfehleranzeigenden Signals ist, um die Länge des gegebenen Intervalles entsprechend diesem Absolutwert zu ändern.

12. Einrichtung nach Anspruch 1, weiterhin gekennzeichnet durch eine Quelle (IS4) eines zweiten Stromes (24), wobei die steuerbare Anordnung den ersten Strom (i3) auf die Kapazität (C4) koppelt, wenn die Phasendifferenz eine erste Polarität hat und den zweiten Strom (i4) auf die Kapazität koppelt, wenn die Phasendifferenz die entgegengesetzte Polarität hat, so daß während eines gegebenen Phasendemodulationszyklus, solange die Phasendifferenz die erste Polarität hat, der zweite Strom (i4) von der Kapazität (C4) abgekoppelt ist, und solange die Phasendifferenz die entgegengesetzte Polarität hat, der erste Strom (i3) von der Kapazität (C4) abgekoppelt ist.

Revendications

1. Appareil décodeur stéréo répondant à un signal composite analogique contenant une information audio qui contient un composant signal pilote, comprenant:
un oscillateur contrôlable (124) répondant à un premier signal de commande analogique (123a), ledit oscillateur produisant un signal d'oscillation à une fréquence qui est réglée en accord avec ledit premier signal de commande;
et caractérisé par
des moyens d'échantillonnage répondant audit signal composite analogique pour échantillonner ledit signal composite pour produire à partir de celui-ci un signal binaire pondéré échantillonné possédant une première pluralité de binaires qui représentent ledit signal composite sous une forme numérique pondérée binaire et qui contient ladite information de synchronisation dudit composant de signal pilote;
un moyen (120) répondant audit signal échantillonné et audit signal d'oscillation pour produire un signal indiquant une erreur de phase (122a) qui forme un mot numérique possédant une deuxième pluralité de binaires avec une valeur numérique pondérée binaire qui indique une différence de phase entre ledit composant de signal pilote et ledit signal d'oscillation;
une source (IS3) d'un premier courant (i3);
une capacité (C4);

des moyens contrôlables (204, 205, ASW1, ASW2, ASW3, ASW4) répondant à un deuxième signal de commande qui est couplé à une borne de commande de celui-ci pour coupler ledit premier courant (i3) à ladite capacité pendant un intervalle donné; et

des moyens (200, 202, 203, 204) répondant à ladite deuxième pluralité de binaires dudit signal indiquant une erreur de phase pour produire ledit deuxième signal de commande de manière à faire varier une longueur dudit intervalle donné pendant lequel ledit premier courant est couplé à ladite capacité de façon à développer ledit premier signal de commande analogique dans ladite capacité.

2. Appareil selon la revendication 1, caractérisé en ce que ledit deuxième moyen de production de signaux de commande comprend un compteur (202) qui est prééglé en accord avec une valeur dudit signal indiquant une erreur de phase, dans lequel ledit compteur (202) qui répond à un signal d'horloge compte les impulsions dudit signal d'horloge pendant ledit intervalle donné, et dans lequel ledit deuxième signal de commande est produit aussi longtemps que ledit compteur compte lesdites impulsions dudit signal d'horloge.
3. Appareil selon la revendication 1, caractérisé en ce que ledit deuxième signal de commande est produit lorsque ledit signal indiquant une erreur de phase est à une première polarité (PLUS) et n'est pas produit lorsque ledit signal indiquant une erreur de phase est à la polarité opposée.
4. Appareil selon la revendication 3, caractérisé en ce que ledit moyen contrôlable qui couple ledit premier courant à ladite capacité (C4) comprend un premier commutateur (ASW1) qui est conducteur lorsque ledit deuxième signal de commande est produit.
5. Appareil selon la revendication 4, caractérisé en outre par un moyen (205) répondant audit signal indiquant une erreur de phase pour produire un troisième signal de commande (DECHARGE) pendant un deuxième intervalle donné qui varie en accord avec ladite valeur dudit signal indiquant une erreur de phase de telle sorte que ledit troisième signal de commande est produit lorsque ledit signal indiquant une erreur de phase est à ladite polarité opposée, et un deuxième commutateur qui est conducteur pendant ledit deuxième intervalle donné lorsque ledit troisième signal de commande est produit pour coupler une source



(IS4) d'un deuxième courant (i4) à ladite capacité (C4) qui change ledit premier signal de commande dans ladite capacité d'une manière opposée à celle dudit premier courant (i3).

6. Appareil selon la revendication 5, caractérisé en outre par un troisième commutateur (ASW2) répondant audit deuxième signal de commande qui est conducteur lorsque ledit premier commutateur (ASW1) n'est pas conducteur, et vice versa, pour former un trajet de courant alternatif audit premier courant (i3) lorsque ledit premier commutateur (ASW1) n'est pas conducteur.

7. Appareil selon la revendication 6, caractérisé en ce que ledit troisième commutateur (ASW2) amène l'écoulement dudit premier courant à être essentiellement ininterrompu lorsque ledit premier commutateur (ASW1) change de l'état conducteur à l'état non conducteur et de l'état non conducteur à l'état conducteur.

8. Appareil selon la revendication 1, caractérisé en ce que ledit oscillateur contrôlable (124) comprend un transistor à effet de champ (124c) dont une électrode de grille est couplée audit premier signal de commande de telle façon qu'une impédance d'entrée élevée dudit transistor à effet de champ empêche qu'une charge dans ladite capacité (C4) change en dehors dudit intervalle donné.

9. Appareil selon la revendication 1, caractérisé en ce que ledit deuxième signal de commande a une durée d'impulsion qui détermine ladite longueur dudit intervalle donné lorsque ledit premier courant est couplé à ladite capacité.

10. Appareil selon la revendication 1, caractérisé en ce que ledit deuxième signal de commande est produit seulement lorsqu'une différence de phase entre ledit composant de signal pilote et ledit signal d'oscillation est à une première polarité.

11. Appareil selon la revendication 1, caractérisé en ce que ledit moyen contrôlable comprend un moyen (200) pour produire un deuxième signal d'indication de phase formant un mot numérique possédant une valeur qui est égale à une valeur absolue dudit premier signal indiquant une erreur de phase pour commander la longueur dudit intervalle donné en accord avec ladite valeur absolue.

12. Appareil selon la revendication 1, caractérisé en outre par une source (IS4) d'un deuxième

courant (24), dans lequel ledit moyen contrôlable couple ledit premier courant (i3) à ladite capacité (C4) lorsque ladite différence de phase est à une première polarité et couple ledit deuxième courant (i4) à ladite capacité lorsque ladite différence de phase est à la polarité opposée de telle sorte que pendant un cycle de détection de phase donné, aussi longtemps que ladite différence de phase est à ladite première polarité, ledit deuxième courant (i4) est découplé de ladite capacité (C4) et, aussi longtemps que ladite différence de phase est à la polarité opposée, ledit premier courant (i3) est découplé de ladite capacité (C4).

