Semiconductor Integrated Circuit Device and Fabrication Method thereof

The present invention relates to a semiconductor integrated circuit device and a method of fabricating the same. Especially, in a specific form of the semiconductor integrated circuit device of the present invention, a linear circuit and an IIL (Integrated Injection Logic) circuit are formed in one semiconductor substrate.

The Inventor, has conceived a semiconductor integrated circuit device (which will be hereinafter referred to as an "IC") having the aforementioned circuit construction for controlling a power source. This power source controlling IC is used in a machining robot, for example, and has such an IC chip plane pattern as is schematically shown in Fig. 1. As shown in Fig. 1, more specifically, that power source controlling IC is composed of an IIL elements portion 2, which is formed in a semiconductor substrate 1 for constructing the IIL circuit,

a linear elements portion 3 which is formed in the semiconductor substrate 1 so as to be arranged around that IIL elements portion 2. Moreover, the IIL elements portion 2 is composed of a high speed IIL elements portion 2a, which is operative at a high speed, and a low speed IIL elements portion 2b which is operative at a low speed. These high and low speed IIL elements portions 2a and 2b constitute a specific logical circuit such as shown in Fig. 2. More specifically, the logical circuit shown in Fig. 2 is composed of an inverter INV and an n number of flip-flop circuits F/F-1, F/F-2, F/F-3, - - - - - -F/F-n connected in cascade, thus forming a frequency dividing circuit. This frequency dividing circuit has its input line A fed with a clock signal of 400 KHz, for example, and its input line B fed with a reset signal. From the output line C of the frequency dividing circuit there is derived a signal which has its frequency divided by the n number of the flip-flop circuits.

The specific circuit of the inverter INV is composed, as shown in Fig. 3a, of a PNP transistor Q_1 and an NPN transistor Q_2 having a plurality of outputs (or collectors) OUT_1 to OUT_3, thus forming

a well-known IIL inverter circuit. More specifically, since the IIL inverter circuit of Fig. 3a can be expressed as a logical circuit shown in Fig. 3b, the inverter INV of Fig. 2 is formed by connecting in common the outputs (or collectors) of the transistor Q_2 of the IIL inverter circuit which is specifically shown in Fig. 3a. The common connection of the output portions of the transistor Q_2 is made to improve the driving capacity of the inverter INV.

Each of the flip-flop circuits F/F-1, F/F-2, F/F-3, - - - - - -F/F-n is composed, as shown in Fig. 4, of a plurality of inverters INV1 to INV 8. Each of the inverters INV1 to INV8 comprises an IIL inverter circuit similar to that shown in Fig. 3a for the inverter INV. One flip-flop circuit F/F shown in Fig. 4 has its trigger terminal T and its reset terminal R fed with a clock signal and a reset signal, respectively. Moreover, an output signal of the flip-flop circuit F/F is derived from an output terminal Q. From an output terminal $\bar{Q}$, on the other hand, there is derived an output signal which is in opposite phase to the signal derived from the output terminal Q. However, that output terminal $\bar{Q}$ is not used in the frequency dividing circuit shown in Fig. 2.

In order to raise the speed and reduce the power consumption of the frequency dividing circuit thus far described, there has been conceived a method for driving the high speed IIL elements portion 2a and the low speed IIL elements portion 2b by different injection currents. For example, in the high speed IIL elements portion (including the inverter INV and the flip-flop circuits F/F-1 and F/F-2) 2a, fed with a clock signal of 400 KHz to 100 KHz, an injection current I_{inj} (i.e., the injection current for one IIL inverter circuit) shown in Fig. 3a is set at 20 to 30 μA so as to make high speed operation possible. In the low speed IIL elements portion (including the flip-flop circuits F/F-3 to F/F-n) 2b fed with a clock signal equal to or lower than 100 KHz, the injection current is reduced, because there is no need for any high speed operation, to 5 to 6 μA so as to minimize the power consumption.

Here, since separate injection current sources are constructed in the IC so as to establish the aforementioned different injection currents, the number of the elements included is increased, and the number of wires for connecting the injection current sources and the IIL element portions is increased, raising the problem that the integration

density of the IC is lowered.

It is, therefore, desirable to provide a semiconductor integrated circuit device which is formed with a highly dense IIL elements portion intended to have a high operating speed and a low power consumption.

In a preferred embodiment there is provided a semiconductor integrated circuit device which is formed with the aforementioned IIL elements portion and a linear elements portion arranged around the former.

A further aspect of the present invention provides a method of fabricating a semiconductor integrated circuit device which is formed with the aforementioned IIL element portion and linear elements portion.

The semiconductor integrated circuit device of the present invention is characterized in that it includes a first IIL elements portion, which is arranged to be operated by a first injection current, and a second IIL elements portion which is arranged to be operated by a second injection current different from said first injection current, in that injection regions for said first and second IIL elements portions are connected with one injection current source, and in that means for establishing said second injection current is connected with or part of the injection region for said second IIL elements portion.

In the accompanying drawings:

Fig. 1 is a top plan view showing the pattern of an IC chip relating to the present invention;

Fig. 2 is a diagram showing a logical circuit (or a frequency dividing circuit) relating to the present invention;

Fig. 3a is a diagram showing an IIL inverter circuit relating to the present invention;

Fig. 3b is a diagram showing the logical circuit of Fig. 3a;

Fig. 4 is a logical circuit diagram showing in more detail a flip-flop circuit of Fig. 2;

Fig. 5 is a top plan view showing a portion of the IC according to one embodiment of the present invention;

Fig. 6 is a schematic circuit diagram of the IC shown in Fig. 5;

Figs. 7a to 7f are sectional views illustrating the fabrication process of the IC shown in Fig. 5;

Figs. 8 to 10 are top plan views showing portions of ICs according to other embodiments of the present invention, respectively;

Fig. 11 is a section taken along line B - B' of Figs. 9 and 10;

Fig. 12 is a top plan view showing a portion of an IC according to a further embodiment of the present invention;

Fig. 13 is a section taken along line C - C' of Fig. 12;

Fig. 14 is a top plan view schematically showing an IC according to a further embodiment of the present invention; and

Fig. 15 is a top plan view showing a portion of an IC according to a further embodiment of the present invention.

Specific embodiments of the invention will now be described with further reference to the drawings.

Fig. 5 is a top plan view showing a portion of an IC according to the present invention and illustrates in detail the IIL elements portion which is composed of the high speed IIL elements portion 2a and the low speed IIL elements portion 2b, as shown in Fig. 2.

In Fig. 5, the reference numeral 1 indicates a semiconductor substrate which is made of silicon and which is formed therein with a ring-shaped semiconductor region 3. The high speed IIL elements portion 2a and the low speed IIL elements portion 2b exist in an island region 4 which is enclosed by that semiconductor region 3. Those IIL elements portions 2a and 2b comprise an elongated injection region 5, which is selectively formed, a plurality of base regions B_1, B_2, - - - - - - B_m, which are formed along both sides of that injection region 5, and a plurality of output regions (or collector regions) OUT_1, OUT_2 and OUT_3 which are selectively formed in those base regions B_1, B_2, - - - - - - B_m. In other words, a plurality

of (i.e., an m number of) IIL inverter circuits, e.g. as in Fig. 3a, are formed by the above-identified regions. For example, the PNP type transistor Q_1 in one IIL inverter circuit shown in Fig. 3a is a transistor having a lateral construction whereby its emitter is the injection region 5, its base is the island region 4 and its collector is the base region B_1; whereas the NPN type transistor Q_2 is a transistor having an inverse construction whereby its emitter is the island region 4, its base is the base region B_1 and its collector comprises output regions OUT_1, OUT_2 and OUT_3.

The points to be noted in the IC shown in Fig. 5 are that the aforementioned high and low speed IIL elements portions 2a and 2b are driven by one injection current source 7, and that the injection current for the low speed IIL elements portion 2b is made different by a resistor portion R from the injection current for the high speed IIL elements portion 2a. In other words, according to the specific IC of the embodiment shown in Fig. 5, separate injection current sources are not provided for the high and low speed elements portions 2a and 2b, respectively.

The injection current source 7 is electrically

connected with an injection portion 5a for the high speed IIL elements portion 2a through a metal layer which is made of a highly conductive metal such as aluminum. Moreover, the injection portion 5a has its surface coated with a metal layer 6a, which is made of a highly conductive metal such as aluminum, so that the injection currents to flow into the respective IIL elements of the high speed IIL elements portion 2a may be uniform.

In the low speed IIL elements portion 2b, there exists the resistor portion which determines the injection current for that low speed elements portion 2b. That resistor portion R makes use of a portion of the injection region 5 and is prepared merely by narrowing a portion of the width of the injection region 5 and by preventing that portion from being coated with the metal layer. However, an injection portion 5b for the low speed IIL elements portion 2b has its surface coated with a metal layer, which is made of a highly conductive metal such as aluminum, so that the injection current to flow into the respective IIL elements of the slow IIL elements portion 2b may be uniform. Furthermore, those metal layers 6a and 6b (i.e., the first wiring layers) are coated with an interlayer insulating film (although

not shown), on which there are formed, for example, second wiring layers La and Lb intersecting the metal layers 6a and 6b, as indicated by thick solid lines. Especially the IC, in which the injection region 5 is formed in a linear shape and which is formed with the IIL elements portion to be commonly used for the plural IIL elements, as shown in Fig. 5, should be of the two-layered wiring construction, as has been described hereinabove, so as to facilitate the wiring layout and to improve the integration density.

Fig. 6 is an IIL circuit diagram showing the IC of Fig. 5 substantially in an equivalent manner.

In Fig. 6, an equal injection current $I_{inj}(a)$ flows through the respective IIL elements (or the IIL inverters) INV, INV_1, - - - - - - INV_{17} in the high speed IIL elements portion 2a because the injection portion 5a has its surface coated with the metal layer 6a. On the other hand, an equal injection current $I_{inj}(b)$ flows through the respective IIL elements INV_{18}, - - - - - -INV_m in the low speed IIL elements portion 2b because the injection portion 5b has its surface coated with the metal layer 6b. Because of the existence of the resistor portion R, however, the

voltage at point B is lower than that at point A. As a result, the injection current $I_{inj}(b)$ is far lower than the injection current $I_{inj}(a)$. Moreover, since most of the IIL elements are formed in the low speed IIL elements portion 2b, even a slight voltage drop at the resistor portion R can considerably reduce the injection current $I_{inj}(b)$ of each of the IIL elements. Specifically, the resistance of that resistor portion R is sufficient if at 10 Ω to 30 Ω.

For this reason thus far described, a sufficiently high injection current (e.g., $I_{inj}(a)$ = 20 to 30 μA) is enabled to flow through the high speed IIL elements portion 2a so that high speed operation can be conducted. On the other hand, a low injection current (e.g., $I_{inj}(b)$ = 5 to 6 μA) is enabled to flow through the low speed IIL elements portion 2b so that the power to be consumed at that portion can be reduced. As has been described hereinbefore, on the other hand, since the high speed IIL elements portion 2a and the low speed IIL elements portion 2b can be driven by the single current source 7, it is unnecessary to provide separate injection current sources for the IIL elements portions. It is, therefore, possible to greatly improve the layout

efficiency and the integration density of the IC.

Next, the method of fabricating the IC shown in Fig. 5 will be described with reference to Figs. 7a to 7f. In Figs. 7a to 7f, the sectional portions at the lefthand side illustrate the fabrication steps of a vertical transistor in the linear elements portion. On the other hand, the sectional portions at the righthand side illustrate the fabrication steps of the IIL elements, especially, the fabrication steps of the IIL elements at the portion taken along line A - A' of Fig. 5. Incidentally, the parenthesized symbols or numerals correspond to those appearing in Fig. 5.

(a) First of all, as illustrated in Fig. 7a, an N-type impurity such as antimony is selectively introduced into a P-type silicon substrate 10 having a specific resistance of 20 to 50 Ωm thereby to form N^+-type regions 11 and 12. Moreover, an N-type impurity having a relatively high diffusion coefficient such as phosphorus is selectively introduced into the N^+-type region 12 so as to increase the current amplification factor of the inverse transistor Q_2 in the IIL elements, thus forming an N^+-type region 13. Incidentally, this N^+-type region 13 may be formed by the ion implantation. After that, the silicon

substrate 10 has its whole surface formed with an N^--type epitaxial layer 14. This epitaxial layer 14 has a specific resistance of 2.5 Ωm and a thickness of about 13 μ.

(b) As shown in Fig. 7b, the epitaxial layer 14 has its surface coated with an insulating film, e.g., a silicon dioxide (SiO_2) film 15 having a thickness of 0.8 μ. This SiO_2 film 15 can be easily formed by thermally oxidizing the surface of the epitaxial layer 14. Moreover, the SiO_2 film 15 is selectively removed, and a P-type impurity such as boron is introduced into the exposed epitaxial layer 14 thereby to form a P^+-type region 16 for isolation. Moreover, the SiO_2 film 15 is selectively removed, and an N-type impurity such as phosphorus is introduced into the exposed epitaxial layer 14 thereby to form an N-type region 17. This N-type region 17 is formed by the ion implantation so as to increase the current amplification factor of the inverse transistor Q_2 similarly to the aforementioned N^+-type region 13.

(c) As shown in Fig. 7c, the SiO_2 film is selectively removed so as to reduce the collector resistance of the transistor constructing the linear circuit, and an N-type impurity (e.g., phosphorus) is introduced into the exposed epitaxial layer 14. By extending

and diffusing that P-type impurity, an N^+-type region 18 to contact with the N^+-type region 11 is formed. In this extending and diffusing operation, the N^+-type regions 11, 12 and 13, the P^+-type region 13 and the N-type region 17 are extended to bring the N^+-type region 16 and the N-type region 17 into contact with each other and to bring the P-type region 16 into contact with the P-type substrate 10. By this contact between the P-type region 16 and the P-type substrate 10, there is formed an island region 19 which is electrically isolated from the linear circuit portion.

(d) As shown in Fig. 7d, a SiO_2 film 15' formed on the surface of the N-type region 17 is selectively removed, and a P-type impurity (e.g., boron) is introduced into the exposed N-type region 17 thereby to form a P^+-type region 20 having a sheet resistance of 13 Ω/□. This P^+-type region 20 forms the injection (or emitter) region of the lateral transistor Q_1 in the IIL element. On the other hand, that P^+-type region 20 is formed simultaneously with the emitter and collector regions (although not shown) of the lateral transistor in the linear elements portion.

(e) As shown in Fig. 7e, the SiO_2 films 15 and 15' are selectively removed, and a P-type impurity (e.g., boron) is introduced into the exposed epitaxial

layer and N-type region 15 and 17 thereby to form P-type regions 21, 22, 23 and 20' having a sheet resistance of 200 Ω/□. The P-type region 21 forms the base region of the vertical transistor in the linear elements portion. On the other hand, the P-type regions 22 and 23 form the collector region of the lateral transistor Q_1 and the base region of the inverse transistor Q_2 both in the IIL elements. As is apparent from the Figure, the P-type region 20' is made so wider than the P^+-type region 20 as to determine the base width of the lateral transistor Q_1 together with the P-type regions 22 and 23. The formation of that P-type region 20' is very important for ensuring a predetermined base width. Specifically, one photoetching mask is used upon the formations of the P-type region 20' and the P-type regions 22 and 23. As a result, there is no dispersion in the base width. Unless the P-type region 20' is formed, the base width of the lateral transistor Q_1 is determined by the P^+-type region 20 and the P-type regions 22 and 23. In this case, however, separate photoetching masks are used to form the P^+-type region 20 and the P-type regions 22 and 23. As a result, the dispersion in the base width is remarkably enlarged by errors in the registration of the masks or the like.

(f) As shown in Fig. 7f, the SiO_2 films formed on the surfaces of the P-type regions 21, 22 and 23 are selectively removed, and an N-type impurity (e.g., phosphorus) is introduced into the exposed P-type regions 21, 22 and 23 thereby to form N^+-type regions 24, 25, 26, 27 and 28. The N^+-type region 24 forms the emitter region of the aforementioned vertical transistor. On the other hand, the N^+-type regions 25, 26, 27 and 28 form the output regions (or the collector regions) of the aforementioned inverse transistor Q_2. After that, electrodes 29 to 38 are formed for the regions 24, 21, 18, 16, 25, 26, 20, 27 and 28, respectively. After that, although not shown, the silicon substrate 10 is coated with an interlayer insulating film made of a material having an excellent moisture-resistance such as polyisoindoquinazolinedione (i.e. a polyimide resin), and a second wiring layer is formed on that interlayer insulating film. The resistor portion R shown in Fig. 5 exists in a portion of the P^+-type region 20 because the electrode is not formed all over the surface of the P^+-type region 20, as is apparent from Fig. 7f.

The IC of Fig. 5 is fabricated by the steps thus far described.

In the method thus far described, incidentally,

the injection region 5 having the resistor portion R is not formed at the step (d) but may be formed at the step (e) simultaneously with the P-type regions 21, 22 and 23.

As is now apparent from the method thus far described, especially the formation of the resistor portion R needs no special additional step but may be easily achieved merely by leaving the surface of the portion of the injection region 20 not coated with the metal layer.

The present invention should not be limited to the embodiment thus far described but may be conceived to have such modifications as will be described in the following, as well as other possible modifications.

(1) The IC shown in Fig. 5 is constructed such that the high speed IIL elements portion and the low speed IIL elements portion are connected in cascade but may be modified such that the high speed IIL elements portion 20 and the low speed IIL elements portion 2b are connected in parallel, as shown in Fig. 8. In the same Figure, incidentally, portions corresponding to those of Fig. 5 are indicated at identical reference symbols and numerals. The IC of Fig. 8 is formed by absolutely the same method as that of the IC of Fig. 5.

(2) Figs. 9 and 10 are top plan views showing the

modified constructions of the IIL elements portion, respectively. Especially, Fig. 9 shows the modified construction of the resistor portion R' formed in the IC, in which the high speed IIL elements portion and the low speed IIL elements portion are connected in cascade, as shown in Fig. 5. On the other hand, Fig. 10 shows the modified construction of the resistor portion R' formed in the IC, in which the high speed IIL elements portion and the low speed IIL elements portion are connected in parallel, as shown in Fig. 8. In Figs. 9 and 10, portions corresponding to those of Fig. 5 are indicated at identical reference symbols and numerals.

A resistor portion R' shown in Figs. 9 and 10 is formed simultaneously with the output regions (or the collector regions) OUT_1 and OUT_2. More specifically, that resistor portion R' is selectively formed in the injection region 5 simultaneously with the N^+-type regions 24, 25, 26, 27 and 28 shown in Fig. 7f. Incidentally, reference letters CH_1, CH_2, CH_3 and CH_4 indicate contact holes which are formed in the insulating film (i.e., the SiO_2 film) 15.

Fig. 11 is a section taken along line B - B' of Figs. 9 and 10. In the same Figure, the injection region 5 is formed simultaneously with the base region

of the vertical transistor in the linear elements portion. However, that injection region 5 may be formed simultaneously with the emitter and collector regions of the lateral transistor in the linear elements portion.

According to the embodiment under consideration, the resistor portion R' and the injection region 5 are inversely biased from the standpoint of their potential because they are made of the N^+-type region and the P-type region, respectively. As a result, the resistor portion R' can be used as the resistor. Moreover, a resistor having a low resistance can be easily formed.

(3) Fig. 12 is a top plan view showing a modified construction of the other IIL elements portion. And, Fig. 13 is a section taken along line C - C' of Fig. 12. In Fig. 12, incidentally, portions corresponding to those of Fig. 5 are indicated at identical reference symbols and numerals.

According to this embodiment, as is apparent from Fig. 12, the injection region 5 and the base regions B_1, B_2, B_3 and B_4 are enclosed by an N^+-type region 100 having a high impurity concentration, which is formed simultaneously with the output regions OUT_1 and OUT_2 except portions where the injection region 5

and the base regions B_1 to B_4 face one another.

The provision of that N^+-type region 100 can reduce the leak of carriers transversely of the injection region 5 and the base regions B_1 to B_4 thereby to further speed up the operation and reduce the power consumption.

(4) As shown in Fig. 14, resistor portions Ra, Rb and Rc having different resistances may be connected with respective injection portions 5a, 5b and 5c so that different injection currents may be established at the respective injection portions 5a, 5b and 5c. Incidentally, those resistor portions Ra, Rb and Rc adopt a variety of constructions, as has been specifically described hereinbefore.

(5) The present invention can also be applied, as shown in Fig. 15, to the IC which is formed with the independent injection regions 5a and 5b for the IIL elements 2a and 2b, respectively. More specifically, the respective IIL elements 2a and 2b are connected with the single injection current source 7 through a metal layer 6, and especially the IIL element 2b adapted to operate at a low speed has its injection region 5b forming the resistor portion R. This resistor portion R can also adopt a variety of such constructions as have been specifically described

hereinbefore.

(6) The resistor portion R thus far described makes use of the semiconductor region, which is formed in the semiconductor substrate, but should not be limited thereto. That resistor portion R may be a semiconductor region such as the polycrystalline silicon which is formed on the surface of the insulating film over the semiconductor substrate. The use of that polycrystalline silicon is effective for the IC which includes an insulated gate type field effect elements portion other than the linear elements portion. Specifically, the polycrystalline silicon used as the resistor portion R can be formed simultaneously with the gate electrode of the insulated gate type field effect elements portion. Incidentally, this insulated gate type field effect elements portion is constructed of an N-channel MISFET, complementary MISFETs or the like.

As has been apparent from the description thus far described, the present invention is effective in the IC having the IIL elements portion and is remarkably effective where the number of the IIL elements in the low speed IIL elements portion 2b is far larger than the number of the IIL elements in the high speed IIL elements portion 2a. This is because the power to be consumed at the low speed IIL elements portion

2b having a large number of the IIL elements can be sufficiently reduced by the existence of the resistor portion R.

CLAIMS:

1. A semiconductor integrated circuit device comprising: a semiconductor substrate; a first IIL elements portion formed in said semiconductor substrate and arranged to be operated by a first injection current; a second IIL elements portion formed in said semiconductor substrate and arranged to be operated by a second injection current different from said first injection current; injection regions for said first and second IIL elements portions being connected with one injection current source; and means for establishing said second injection current being part of or connected with at least the injection region for said second IIL elements portion.

2. A semiconductor integrated circuit device according to claim 1 having one semiconductor substrate in which are formed a linear elements portion and an IIL elements portion which includes said first and second IIL elements portions.

3. A semiconductor integrated circuit device according to claim 1 or claim 2, wherein said second IIL elements portion is arranged to be operated at a lower speed than said first IIL elements portion, and wherein said second injection current is lower than said first injection current.

4. A semiconductor integrated circuit device according to any one of claims 1, 2 and 3, wherein the means for establishing said second injection current is provided by a semiconductor layer which is formed on the surface of an insulating film over said semiconductor substrate.

5. A semiconductor integrated circuit device according to any one of the preceding claims, wherein the means for establishing said second injection current is provided by a portion of said second injection region which is not coated with a metal layer.

6. A semiconductor integrated circuit device according to any one of claims 1 to 4, wherein at least the second injection region has a portion coated with metal to provide uniform current to the IIL elements connected therewith, and the means for establishing said second injection current is provided by a portion of said injection region which is not coated with the metal layer.

7. A semiconductor device substantially as described herein with reference to the drawings.

8. A method of fabricating a semiconductor integrated circuit device, comprising:

the step of preparing a semiconductor substrate having first and second semiconductor regions of first

conduction type isolated from each other;

the step of selectively forming an elongated third semiconductor region of second conduction type exhibiting the opposite conduction type to said first conduction type in said second semiconductor region;

the step of selectively forming both a fourth semiconductor region of said second conduction type in said first semiconductor region and a plurality of fifth semiconductor regions of said second conduction type in said first semiconductor region along said third semiconductor region;

the step of selectively forming both a sixth semiconductor region of said first conduction type in said fourth semiconductor region and a plurality of seventh semiconductor regions of said first conduction type in said plural fifth semiconductor regions, respectively; and

the step of coating both the surface of a first portion of said third semiconductor region and the surface of a second portion of the same, which is spaced from said first portion, with a metal layer,

wherein a transistor of a linear elements portion is constructed of said first semiconductor region, said fourth semiconductor region and said sixth semiconductor region,

wherein a first IIL element is constructed of said second semiconductor region, the first portion of said third semiconductor region, and said fifth and seventh semiconductor regions formed along said first portion, and

wherein a second IIL element is constructed of said second semiconductor region, the second portion of said third semiconductor region, and said fifth and seventh semiconductor regions formed along said second portion.

9. A method of fabricating a semiconductor integrated circuit device of any one of claims 1 to 7, substantially as described herein with reference to the accompanying drawings.