CLAIMS

1. A semiconductor device, comprising:

a hybrid channel region comprising a nanowire portion disposed above an omega FET portion disposed above a fin-FET portion;

a gate stack disposed on exposed surfaces of the hybrid channel region, the gate stack comprising a gate dielectric layer and a gate electrode disposed on the gate dielectric layer, the gate stack completely separating the nanowire portion from the omega FET portion of the hybrid channel region; and

source and drain regions disposed on either side of the hybrid channel region.

2. The semiconductor device of claim 1, wherein the nanowire portion and the fin-FET portion of the hybrid channel region consist essentially of a first semiconductor material, and wherein the omega-FET portion comprises a bi-layer comprising an upper layer consisting essentially of the first semiconductor material and a lower layer consisting essentially of a second, different, semiconductor material.

3. The semiconductor device of claim 2, wherein the first semiconductor material is silicon, and the second semiconductor material is silicon germanium.

4. The semiconductor device of claim 2, wherein the lower layer of the omega-FET portion of the hybrid channel region is disposed on the fin-FET portion of the hybrid channel region.

5. The semiconductor device of claim 1, wherein the fin-FET portion of the hybrid channel region is continuous with a bulk semiconductor substrate.

6. The semiconductor device of claim 5, wherein the gate stack is isolated from the bulk semiconductor substrate by a shallow trench isolation (STI) region or a bottom gate isolation (BGI) structure.

7. A semiconductor device, comprising:

a hybrid channel region comprising a first region disposed above a second region disposed above and spaced apart from a third region, and comprising a fourth region disposed

between and in contact with the first and second regions, wherein the first region, the second region and the third region consist essentially of a first semiconductor material, and wherein the fourth region consists essentially of a second, different, semiconductor material;

a gate stack disposed on exposed surfaces of the hybrid channel region, the gate stack comprising a gate dielectric layer and a gate electrode disposed on the gate dielectric layer, the gate stack completely separating the second region from the third region of the hybrid channel region; and

source and drain regions disposed on either side of the hybrid channel region.

8. The semiconductor device of claim 7, wherein the first semiconductor material is silicon, and the second semiconductor material is silicon germanium.

9. The semiconductor device of claim 7, wherein the hybrid channel region has a length between the source and drain regions, and wherein the fourth semiconductor region is shorter than each of the first, second, and third semiconductor regions in a direction perpendicular to the length of the channel region.

10. The semiconductor device of claim 7, wherein the third region of the hybrid channel region is continuous with a bulk semiconductor substrate.

11. The semiconductor device of claim 10, wherein the gate stack is isolated from the bulk semiconductor substrate by a shallow trench isolation (STI) region or a bottom gate isolation (BGI) structure.

12. A semiconductor device, comprising:

a hybrid channel region comprising a first region disposed above and spaced apart from a second region disposed above a third region, and comprising a fourth region disposed between and in contact with the second and third regions, wherein the first region, the second region and the third region consist essentially of a first semiconductor material, and wherein the fourth region consists essentially of a second, different, semiconductor material;

a gate stack disposed on exposed surfaces of the hybrid channel region, the gate stack comprising a gate dielectric layer and a gate electrode disposed on the gate dielectric layer, the

gate stack completely separating the first region from the second region of the hybrid channel region; and

source and drain regions disposed on either side of the hybrid channel region.

13. The semiconductor device of claim 12, wherein the first semiconductor material is silicon, and the second semiconductor material is silicon germanium.

14. The semiconductor device of claim 12, wherein the hybrid channel region has a length between the source and drain regions, and wherein the fourth semiconductor region is shorter than each of the first, second, and third semiconductor regions in a direction perpendicular to the length of the channel region.

15. The semiconductor device of claim 12, wherein the third region of the hybrid channel region is continuous with a bulk semiconductor substrate.

16. The semiconductor device of claim 15, wherein the gate stack is isolated from the bulk semiconductor substrate by a shallow trench isolation (STI) region or a bottom gate isolation (BGI) structure.

17. A method of fabricating a hybrid geometry-based semiconductor structure, the method comprising:

forming an epitaxial material stack above a semiconductor substrate, the epitaxial material stack comprising a first layer formed above a second layer formed above a third layer formed above a fourth layer formed on the semiconductor substrate, wherein the first layer, the third layer and the semiconductor substrate consist essentially of a first semiconductor material, wherein the second layer consists essentially of a second semiconductor material different than the first semiconductor material, and wherein the fourth layer consists essentially of a third semiconductor material different than the first and second semiconductor materials;

patterning the epitaxial material stack and a portion of the semiconductor substrate to form a semiconductor fin;

exposing the semiconductor fin to an etchant to completely remove one of the second and third semiconductor materials and to only partially remove the other of the second and third semiconductor materials selective to the first semiconductor material; and, subsequently,

forming a gate electrode stack on the semiconductor fin, with source and drain regions on either side of the gate electrode stack.

18. The method of claim 17, wherein exposing the semiconductor fin to the etchant comprises completely removing the second layer of the epitaxial material stack, and wherein the first semiconductor material is silicon, the second semiconductor material is Si_yGe_{1-y}, and the third semiconductor material is Si_xGe_{1-x}, where x>y.

19. The method of claim 17, wherein exposing the semiconductor fin to the etchant comprises completely removing the fourth layer of the epitaxial material stack, and wherein the first semiconductor material is silicon, the third semiconductor material is Si_yGe_{1-y}, and the second semiconductor material is Si_xGe_{1-x}, where x>y.

20. The method of claim 17, wherein exposing the semiconductor fin to the etchant comprises wet etching with a composition selected from the group consisting of an aqueous carboxylic acid/nitric acid/HF solution and an aqueous citric acid/nitric acid/HF solution.

21. The method of claim 17, wherein forming the gate electrode stack comprises using a replacement gate process.