CLAIMS

We claim:

1. An apparatus comprising:

a capacitor having a first terminal and a second terminal;

a first transistor having a gate terminal coupled to a first word line (WL), a source/drain terminal coupled to bit line (BL), and drain/source terminal coupled to the first terminal of the capacitor;

a resistive memory element having a first terminal and a second terminal, the first terminal of the resistive memory element device coupled to the first terminal of the capacitor; and

a second transistor having a gate terminal coupled to a second WL, a source/drain terminal coupled to source line (SL), and drain/source terminal coupled to the second terminal of the resistive memory element device.

2. The apparatus of claim 1 further comprises control logic for operating the apparatus in DRAM mode or MRAM mode.

3. The apparatus of claim 2, wherein the first transistor when turned ON in DRAM mode, charges the capacitor.

4. The apparatus of claim 3, wherein the second transistor is turned OFF in DRAM mode.

5. The apparatus of claim 2, wherein the first and second transistors are turned ON in MRAM mode.

6. The apparatus of claim 5, wherein the BL and SL are raised and lowered respectively or visa versa to write a state in the resistive memory element.

7. The apparatus of claim 1, wherein the capacitor is a MIM capacitor.

8. The apparatus of claim 1, wherein the resistive memory element is one of:

Magnetic Tunnel Junction (MTJ) device;

Phase Change Memory (PCM) device;

Resistive RAM device; or

Conductive Bridging RAM.

9. An apparatus comprising:

a DRAM bit-cell; and

an MRAM bit-cell integrated with the DRAM bit-cell, wherein a combination of DRAM bit-cell and MRAM bit-cell have no more than four control lines.

10. The apparatus of claim 9, wherein the DRAM bit-cell includes a MIM capacitor.

11. The apparatus of claim 9, wherein the DRAM bit-cell comprises:

a capacitor having a first terminal and a second terminal; and

a first transistor having a gate terminal coupled to a first word line (WL), a source/drain terminal coupled to bit line (BL), and drain/source terminal coupled to the first terminal of the capacitor.

12. The apparatus of claim 11, wherein the MRAM bit-cell comprises:

a resistive memory element having a first terminal and a second terminal, the first terminal of the resistive memory element device coupled to the first terminal of the capacitor; and

a second transistor having a gate terminal coupled to a second WL, a source/drain terminal coupled to source line (SL), and drain/source terminal coupled to the second terminal of the resistive memory element device.

13. The apparatus of claim 12, wherein the four control lines are the first WL, the second WL, SL, and BL.

14. The apparatus of claim 12, wherein the resistive memory element is one of:

Magnetic Tunnel Junction (MTJ) device;

Phase Change Memory (PCM) device;

Resistive RAM device; or

Conductive Bridging RAM.

15. A system comprising:

a processor;

a memory coupled to the processor, the memory having an apparatus according to any one of apparatus claims 1 to 8; and

a wireless interface for allowing the processor to communicate with another device.

16. The system of claim 15 further comprises a display unit.

17. A system comprising:

a processor;

a memory coupled to the processor, the memory having an apparatus according to any one of apparatus claims 9 to 14; and

a wireless interface for allowing the processor to communicate with another device.

18. The system of claim 17 further comprises a display unit.

19. A method comprising:

forming a first transistor having source region, drain region, and gate region;

forming a MIM capacitor and coupling it to the source region of the first transistor;

forming a second transistor having source region, drain region, and gate region;

forming source line (SL) and bit line (BL) in metal zero (M0);

forming a resistive memory element in a region dedicated for metal one (M1) or metal two (M2); and

coupling the resistive memory element to the second transistor and to the first transistor.

20. The method of claim 19, wherein the resistive memory element is one of:

Magnetic Tunnel Junction (MTJ) device;

Phase Change Memory (PCM) device;

Resistive RAM device; or

Conductive Bridging RAM.

CLAIMS

We claim:

1. An apparatus comprising:

a capacitor having a first terminal and a second terminal;

a first transistor having a gate terminal coupled to a first word line (WL), a source/drain terminal coupled to bit line (BL), and drain/source terminal coupled to the first terminal of the capacitor;

a resistive memory element having a first terminal and a second terminal, the first terminal of the resistive memory element device coupled to the first terminal of the capacitor; and

a second transistor having a gate terminal coupled to a second WL, a source/drain terminal coupled to source line (SL), and drain/source terminal coupled to the second terminal of the resistive memory element device.

2. The apparatus of claim 1 further comprises control logic for operating the apparatus in DRAM mode or MRAM mode.

3. The apparatus of claim 2, wherein the first transistor when turned ON in DRAM mode, charges the capacitor.

4. The apparatus of claim 3, wherein the second transistor is turned OFF in DRAM mode.

5. The apparatus of claim 2, wherein the first and second transistors are turned ON in MRAM mode.

6. The apparatus of claim 5, wherein the BL and SL are raised and lowered respectively or visa versa to write a state in the resistive memory element.

7. The apparatus of claim 1, wherein the capacitor is a MIM capacitor.

8. The apparatus of claim 1, wherein the resistive memory element is one of:

Magnetic Tunnel Junction (MTJ) device;

Phase Change Memory (PCM) device;

Resistive RAM device; or

Conductive Bridging RAM.

9. An apparatus comprising:

a DRAM bit-cell; and

an MRAM bit-cell integrated with the DRAM bit-cell, wherein a combination of DRAM bit-cell and MRAM bit-cell have no more than four control lines.

10. The apparatus of claim 9, wherein the DRAM bit-cell includes a MIM capacitor.

11. The apparatus of claim 9, wherein the DRAM bit-cell comprises:

a capacitor having a first terminal and a second terminal; and

a first transistor having a gate terminal coupled to a first word line (WL), a source/drain terminal coupled to bit line (BL), and drain/source terminal coupled to the first terminal of the capacitor.

12. The apparatus of claim 11, wherein the MRAM bit-cell comprises:

a resistive memory element having a first terminal and a second terminal, the first terminal of the resistive memory element device coupled to the first terminal of the capacitor; and

a second transistor having a gate terminal coupled to a second WL, a source/drain terminal coupled to source line (SL), and drain/source terminal coupled to the second terminal of the resistive memory element device.

13. The apparatus of claim 12, wherein the four control lines are the first WL, the second WL, SL, and BL.

14. The apparatus of claim 12, wherein the resistive memory element is one of:

Magnetic Tunnel Junction (MTJ) device;

Phase Change Memory (PCM) device;

Resistive RAM device; or

Conductive Bridging RAM.

15. A system comprising:

a processor;

a memory coupled to the processor, the memory having an apparatus which comprises:

a capacitor having a first terminal and a second terminal;

a first transistor having a gate terminal coupled to a first word line (WL), a source/drain terminal coupled to bit line (BL), and drain/source terminal coupled to the first terminal of the capacitor;

a resistive memory element having a first terminal and a second terminal, the first terminal of the resistive memory element device coupled to the first terminal of the capacitor; and

a second transistor having a gate terminal coupled to a second WL, a source/drain terminal coupled to source line (SL), and drain/source terminal coupled to the second terminal of the resistive memory element device; and

a wireless interface for allowing the processor to communicate with another device.

16. The system of claim 15 further comprises a display unit.

17. The system of claim 15 further comprises control logic for operating the apparatus in DRAM mode or MRAM mode.

18. A system comprising:

a processor;

a memory coupled to the processor, the memory having an apparatus which comprises:

a DRAM bit-cell; and

an MRAM bit-cell integrated with the DRAM bit-cell, wherein a combination of DRAM bit-cell and MRAM bit-cell have no more than four control lines; and

a wireless interface for allowing the processor to communicate with another device.

19. The system of claim 18 further comprises a display unit.

20. The system of claim 18, wherein the DRAM bit-cell includes a MIM capacitor.