

**Method for polishing a semiconductor wafer and polished
semiconductor wafer producible according to the method**

The invention relates to a method for polishing a semiconductor
5 wafer, in particular a silicon semiconductor wafer, which is
intended to provide a semiconductor wafer having an improved
planarity, especially in the edge region, which has not yet
been achievable. The invention relates specifically to a method
for polishing a semiconductor wafer between an upper polishing
10 plate and a lower polishing plate, the semiconductor wafer
being polished on both sides while lying in a recess of a
carrier by supplying a polishing agent, and to a semiconductor
wafer, in particular a silicon semiconductor wafer, having an
improved planarity expressed in the form of the SFQR value and
15 the SBIR value.

The planarity of the semiconductor wafer is a central quality
parameter for assessing the basic suitability of the
semiconductor wafer as a substrate for producing electronic
20 components of the most modern generation. An ideally plane
semiconductor wafer having entirely plane side surfaces lying
mutually parallel would cause no focusing difficulties for the
stepper during the lithography for producing components.
Attempts are therefore made to approximate this ideal shape as
25 far as possible. To this end a semiconductor wafer cut from the
crystal is subjected to a series of processing steps, and in
particular the mechanical processing placed at the start of the
process serves to shape the side surfaces by lapping and/or
grinding. Subsequent steps, such as etching the semiconductor
30 wafer and polishing the side surface, are carried out primarily
to remove superficial damage which the mechanical processing
steps have imparted, and to smooth the side surfaces. At the
same time, these subsequent steps crucially affect the
planarity of the semiconductor wafer and all efforts are aimed
35 at preserving as far as possible the planarity achieved by the

mechanical processing steps. It is known that this object can best be achieved by the incorporation of simultaneously performed double-sided polishing of the semiconductor wafer, referred to below as DSP polishing. A machine suitable for a DSP polishing is described, for example, in DE 100 07 390 A1. During the DSP polishing, the semiconductor wafer lies in a recess intended therefor of a carrier acting as a guide cage, and between an upper polishing plate and a lower polishing plate. At least one polishing plate and the carrier are rotated and the semiconductor wafer is moved, while supplying a polishing agent, on a path predetermined by a milling curve relative to the polishing plates covered with polishing cloth. The polishing pressure, with which the polishing plates press onto the semiconductor wafer, and the duration of the polishing are parameters which jointly determine crucially the material abrasion caused by the polishing.

DE 199 56 250 C1 describes a method in which a mechanically processed and etched silicon semiconductor wafer is subjected first to DSP polishing and subsequently to quality control, in which the planarity is tested and compared with a setpoint value. If the required planarity has not yet been achieved, it is repolished by further, shorter DSP polishing.

According to WO 00/47369, DSP polishing is carried out in a first polishing step in order to give the semiconductor wafer a concave shape, differing from the ideal shape. The concave shape of the polished side surface is removed by a subsequent one-sided polishing, referred to below as CMP polishing. This exploits the fact that CMP polishing applied to a plane side surface tends to impart a convexly polished side surface, and the CMP polishing can produce a plane side surface if the side surface to be polished is shaped concavely.

As the inventors of the present invention have established, the method mentioned above has the disadvantage that only an insufficient planarity of the side surface can be achieved thereby in the region of the wafer edge. The CMP polishing thus
5 reduces the local planarity already achieved by the DSP polishing in this region. The region of the wafer edge is becoming ever more important for the producers of electronic components, however, since attempts are being made to extend the usable area of the polished side surface, referred to below
10 as FQA, fixed quality area, at the cost of a conventional edge exclusion, referred to below as EE. In particular the edge roll-off, referred to below as ERO, is responsible for non-planarity of the side surface in the edge region of the semiconductor wafer. Kimura et al., Jpn. J. Appl. Phys. Vol. 38
15 (1999) pp. 38-39 have shown that the ERO can be derived from the SFQR value of the partial sites. The SFQR value describes the local planarity in a measurement field with a particular size, for example an area of 20 mm x 20 mm, and specifically in the form of the maximum height deviation of the front side of
20 the semiconductor wafer from a reference surface of the same size obtained by least squares minimization. Partial sites are measurement fields in the edge region which are no longer fully part of the FQA, but whose center still lies in the FQA. The SFQR value of the partial sites will be referred to below as
25 the PSFQR value.

Besides the local planarity, at the same time it is still also necessary to consider the global planarity, especially since CMP polishing in the course of producing components demands
30 good global planarity. Standardized parameters for such evaluation are the GBIR value and the SBIR value, which is correlated therewith. Both values express the maximum height deviation of the front side relative to a back side of the semiconductor wafer, assumed to be ideally plane, and differ in
35 that the FQA is used for calculation in the case of the GBIR

value and the area restricted to the measurement field is used for calculation in the case of the SBIR value. Should the definitions given here differ from those of the SEMI standards, especially standards M59, M1 and M1530 in the current version, then the definitions of the standards should take precedence.

It is an object of the present invention to provide a method for polishing a semiconductor wafer which improves the planarity of the semiconductor wafer overall, but without this being done unduly at the cost of the global planarity or the local planarity, especially in the edge region of the semiconductor wafer.

The invention relates to a method for polishing a semiconductor wafer between an upper polishing plate and a lower polishing plate, the semiconductor wafer being polished on both sides while lying in a recess of a carrier by supplying a polishing agent, comprising double-sided polishing of the semiconductor wafer in a first polishing step, which is concluded with a negative overhang, the overhang being the difference between the thickness of the semiconductor wafer and the thickness of the carrier after the first polishing step, and double-sided polishing of the semiconductor wafer in a second polishing step, in which less than 1 μm of material is polished from the side surfaces of the semiconductor wafer.

With this method the local planarity achieved after the first polishing step, particularly in the edge region, can be preserved in the second polishing step and the global planarity can be improved, which leads overall to a planarity that satisfies the requirements of the component generation with a 32 nm line width. This is a surprising result, since the method described in the aforementioned DE 199 56 250 C1 and the method described in the aforementioned WO 00/47369 are not capable of

this. Although in the case of DE 199 56 250 C1 the local planarity set up in the first polishing step is preserved after the second polishing step, the global planarity achieved in the first polishing step is however reduced in the second polishing step. In the case of WO 00/47369 the local planarity achieved by the first polishing step, particularly in the edge region, is reduced by the second polishing step.

A silicon semiconductor wafer produced by the method according to the invention has a planarity which could not previously be achieved. The invention therefore also relates to a silicon semiconductor wafer having a polished front side and a polished rear side with a front side global planarity expressed by an SBIRmax value of less than 100 nm, and with a front side local planarity expressed by a PSFQR value of 35 nm or less in an edge region, an edge exclusion of 2 mm being considered in each case. The SBIRmax value is furthermore related to a measurement field area of 26 x 33 mm and an arrangement of the measurement field grid with offsets of 13 and 16.5 mm in the x and y directions. The SBIRmax value describes the SBIR value of the measurement field with the greatest value among all the measurement fields. The specification of the PSFQR value relates to a measurement field area of 20 x 20 mm and an arrangement of the measurement field grid with an offset of 10 mm in both the x and y directions. The PSQR value is given by the sum of the PSFQR values of the partial sites divided by their number.

The starting product of the method is preferably a semiconductor wafer cut from a crystal, in particular from a silicon single crystal, which has been mechanically processed by lapping and/or grinding the side surfaces i.e. the front and rear sides of the semiconductor wafer. The front side refers to the side surface which is intended to form the surface for providing structured electronic components. The edge of the

semiconductor wafer may already be rounded, in order to make it less sensitive to impact damage. Superficial damage due to the previous mechanical processing has furthermore been substantially removed by etching in an acidic and/or alkaline etchant. Furthermore, the semiconductor wafer may already have been subjected to further processing steps, in particular cleaning steps or polishing the edge. According to the claimed method the semiconductor wafer is polished simultaneously on both sides in a first polishing step, in which case in order to increase the productivity, the DSP polishing is preferably carried out as multi-wafer polishing in which a plurality of carriers are used, each with a plurality of recesses for semiconductor wafers. A particular feature of the first DSP polishing is that a negative overhang is achieved, the overhang being the difference $D1W - D1L$ between a thickness $D1W$ of the semiconductor wafer after polishing has been concluded and a thickness $D1L$ of the carrier used for polishing the semiconductor wafer. The overhang is preferably less than $0\text{ }\mu\text{m}$ to $-4\text{ }\mu\text{m}$, particularly preferably -0.5 to $-4\text{ }\mu\text{m}$, and preferably from $15\text{ }\mu\text{m}$ to $30\text{ }\mu\text{m}$ of material is abraded from the side surfaces overall. The effect of the first polishing step is that the semiconductor wafer is curved concavely in a horizontally symmetrical way, so that the SBIR values lie in an unfavorably regarded range of more than 100 nm , and the SFQR values describing the local planarity, particularly the PSFQR values of the semiconductor wafer already lie in a favorably regarded range of 35 nm or less. The aim of the second polishing step, which is likewise carried out as DSP polishing, is to improve the global planarity and to preserve or likewise improve the local planarity already achieved, especially that in the edge region. A particular feature of the second DSP polishing is that the desired effect is achieved by polishing less than $1\text{ }\mu\text{m}$ of material overall from the two sides of the semiconductor wafer. The averaged material abrasion lies in the range of less than $1\text{ }\mu\text{m}$, preferably in a range of from $0.2\text{ }\mu\text{m}$

to less than 1 μm . The indicated upper limit should not be exceeded because this would detrimentally affect the global planarity of the semiconductor wafer. It is furthermore preferable to achieve an overhang which is $\geq 0 \mu\text{m}$, the overhang being the difference $D2W - D2L$ between a thickness $D2W$ of the semiconductor wafer after the polishing has been concluded and a thickness of the carrier $D2L$ used for polishing the semiconductor wafer. The overhang is particularly preferably from 0 to 2 μm . The effect of the second polishing step is that the SBIR values lie in a favorably regarded range of less than 100 nm, and that the SFQR values describing the local planarity, and in particular the PSFQR values, lie in a favorably regarded range of 35 nm or less.

After the first polishing step, according to a preferred embodiment of the invention, the semiconductor wafer's concavity thereby achieved is determined, for example by measuring the GBIR value. The measured value is used as an input value for calculating the duration of the second polishing step, via which the material abrasion to be achieved by the second polishing step is in turn established. In this way, the planarity of the semiconductor wafer is further optimized. The optimal duration D of the second polishing step is preferably calculated according to the formula: $D = (\text{GBIR} : \text{RT}) + \text{Offset}$, where RT is the typical abrasion rate in $\mu\text{m}/\text{min}$ of the polishing machine being used and Offset is a correction value which depends on the polishing process being used and therefore needs to be determined empirically.

The invention will be explained in more detail below with the aid of figures and comparative examples.

Figure 1 schematically shows the semiconductor wafer lying between the polishing plates at various times in the method. At a time a) at the start of the first DSP polishing, the

semiconductor wafer 1 has a thickness DW which is greater than a thickness D1L of the carrier 21. The semiconductor wafer is polished in the first polishing step between an upper polishing plate 3 and a lower polishing plate 4 by using a particular polishing pressure and supplying a polishing agent, until a time b) is reached at which the difference between the thickness D1W of the polished semiconductor wafer and the thickness D1L of the carrier 21 has become negative. The semiconductor wafer is subsequently subjected to the second DSP polishing with a carrier 22, which is concluded at a time c).

The different effects of the first and second polishing steps are represented in Figs 2 and 3, which show line scans along a diameter of the semiconductor wafer. After the first polishing step (Fig. 2), the semiconductor wafer has a concave shape which is essentially attributable to raised material in a region which extends to about 100 mm inward. Only a slight edge roll-off still exists at the outer edge of the FQA. The consequence of the concavity of the semiconductor wafer is that the global planarity is unsatisfactory. This changes after the second polishing step (Fig. 3) which utilizes an initial effect of double-sided polishing, namely that raised material detrimentally affecting the global planarity is preferentially removed and the local planarity in the edge region thereof remains substantially unaffected.

Examples and comparative examples:

Silicon semiconductor wafers having a diameter of 300 mm were cut from a single crystal and respectively pretreated in the same way by mechanical processing and etching. They were subsequently polished in a type AC 2000 double-sided polishing machine from Peter Wolters AG, until a negative overhang (underhang) had been reached (Example E and comparative example

C2) or until a positive overhang (comparative example C1) had been reached. Some of the semiconductor wafers (C1) were subsequently subjected to a second DSP polishing, which was concluded with a positive overhang and material abrasion of more than 1 μm . Other semiconductor wafers (C2) were subjected to CMP polishing, which was concluded with material abrasion of less than 1 μm . The rest of the semiconductor wafers (E) were likewise subjected to a second DSP polishing, which was concluded with material abrasion of less than 1 μm . The results of planarity measurements, which were carried out with a type AFS contactlessly measuring meter from ADE Corp. after the polishing steps, are collated in the following table.

Parameters for the SBIR and SFQR measurements:

FQA = 296 mm

EE = 2 mm

Parameters for the SBIR measurements:

Measurement field area = 26 mm x 33 mm

Offset of the grid field in the x direction = 13 mm

Offset of the grid field in the y direction = 16.5 mm

Parameters for the PSFQR measurements:

Measurement field area = 20 mm x 20 mm

Offset of the grid field in the x direction = 10 mm

Offset of the grid field in the y direction = 10 mm

Table:

	First polishing step				
	Material abrasion [μm]	Overhang [μm]	GBIR [μm]	SBIRmax [μm]	PSFQR [μm]
C1	26.8	+1.3	0.51	0.27	0.090
C2, E	27.6	-2.7	0.78	0.19	0.034
	Second polishing step				
	Material abrasion [μm]	Overhang [μm]	GBIR [μm]	SBIRmax [μm]	PSFQR [μm]
C1	4.3	+1.0	0.76	0.43	0.060
C2	0.3	-----	0.93	0.23	0.059
E	0.72	0.56	0.111	0.08	0.035

Patent Claims:

1. A method for polishing a semiconductor wafer between an upper polishing plate and a lower polishing plate, the
5 semiconductor wafer being polished on both sides while lying in a recess of a carrier by supplying a polishing agent, comprising
double-sided polishing of the semiconductor wafer in a first polishing step, which is concluded with a negative overhang,
10 the overhang being the difference between the thickness of the semiconductor wafer and the thickness of the carrier after the first polishing step, and
double-sided polishing of the semiconductor wafer in a second polishing step, in which less than 1 μm of material is polished
15 from the side surfaces of the semiconductor wafer.
2. The method as claimed in claim 1, wherein the first polishing step is concluded with a negative overhang of less than 0 μm to -4 μm .
20
3. The method as claimed in claim 1 or claim 2, wherein from 0.2 μm to less than 1 μm of material is polished from the side surfaces of the semiconductor wafer in the second polishing step.
25
4. The method as claimed in one of claims 1 to 3, wherein the concavity of the semiconductor wafer is measured after the first polishing step and the polishing abrasion carried in the second polishing step is made dependent on the measured
30 concavity.
5. A silicon semiconductor wafer having a polished front side and a polished rear side with a front side global planarity expressed by an SBIR_{max} value of less than 100 nm, and with a
35 front side local planarity expressed by a PSFQR value of 35 nm

or less in an edge region, an edge exclusion of 2 mm being considered in each case.

6. The semiconductor wafer as claimed in claim 5, having a
5 diameter of 200 mm or 300 mm.